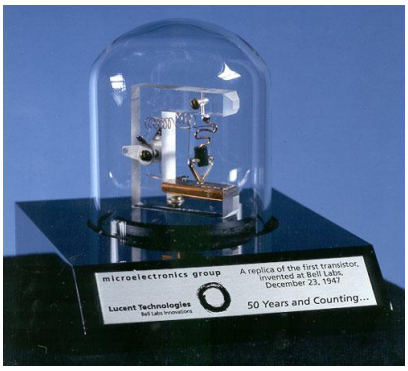



The picture above shows the replica of the first transistor created by Lucent Technologies in 1997, to commemorate the 50th anniversary of the invention of the transistor. Transistors are used in a wide range of applications. You will learn about their basic physics in this unit.

Source of the picture: https://en.wikipedia.org/ https://clintonwhitehouse4.archives.gov/Initiatives/Millennium/capsule/mayo.html

UNIT 3

# TRANSISTORS

## Structure



## STUDY GUIDE

In this unit, you will learn about transistors, which are essentially devices comprising two *p-n* junctions and are called **double junction devices**. You have studied about the bipolar junction transistor in your senior secondary school physics courses in detail. So, you are familiar with the construction, working and biasing conditions of the bipolar junction transistor. In this unit, you will also learn about the field effect transistor. You have to focus on how these devices are constructed, and the physics underlying their working. Then you will learn the contents of the next unit better, which describes various *I-V* characteristic curves of the BJT that lead to its applications as an amplifier and a switch. You should revise Sec. 2.2 of Unit 2 related to the biasing and working of the *p-n* junction diode to learn these concepts well. Note down your difficulties if you do not understand any part of the explanation, and ask your Counsellor to clarify those. You should try to answer all SAQs and Terminal Questions on your own for better learning of the concepts of this unit.

| | |
|---|---|
| ***"Somewhere, something incredible is waiting to be known."*** | ***Carl Sagan*** |

# 3.1 INTRODUCTION

In Unit 2, you have learnt about semiconductor devices called **junction diodes** such as the *p-n* junction diode, the zener diode, LED, solar cell and the photodiode. You have learnt that by adjusting the doping and the construction of the *p-n* junctions, these diodes could be used in a wide variety of applications. In this unit, you will learn how the use of two *p-n* junctions in a single device alters its working, and characteristics that makes it even more useful. Such devices are called **double junction devices**.

In this unit, you will learn about two such devices: **bipolar junction transistor** named so because both electrons and holes carry current in it (*bi* means two); and the **field effect transistor**, which is *unipolar* because current flow in it is due only to one type of charge, electrons or holes (*uni* means one).

Both types of transistors have numerous applications in modern electronic devices and systems as amplifiers and switches. Devices and systems, which involve amplifying signals, such as radio, television, audio systems, satellites and communication systems, space vehicles, power systems, signal generators, etc. use transistors as the basic building blocks. In the form of switching devices, these can be used for many applications such as in logic gates, microprocessors in automatic washing machines, calculators or computers, microcontrollers used for process control in industries, and even to regulate vehicular traffic on the roads.

Transistors are an integral part of the integrated chips (ICs) and mother boards used in various appliances and gadgets around us such as electronic lighters, toys, microwave ovens, modern refrigerators, smart watches, computers, mobile phones, etc. In fact, their use is consistently increasing. You will learn about these applications as you study this unit and the next blocks.

Transistors have brought about a revolution, which has helped upgrade technology and improve efficiency. It is, therefore, important that you understand the basic physics underlying the construction and working of these devices so that you understand how they work as amplifiers and switches. In Secs. 3.2 and 3.3, you will learn about the construction, biasing and working of bipolar junction transistors and junction field effect transistors, respectively. This knowledge will help you understand the *I-V* characteristics of BJTs under different biasing conditions, which we discuss in the next unit.

## Expected Learning Outcomes

After studying this unit, you should be able to:

- describe the construction of bipolar junction transistors and junction field effect transistors;
- explain the biasing and working of bipolar junction transistors; and
- explain the biasing and working of junction field effect transistors.

# 3.2 BIPOLAR JUNCTION TRANSISTOR

The first bipolar junction transistor (BJT) was invented in 1948 by William Shockley, American physicist and inventor (read the margin remark). In this section, we discuss the construction, working and biasing conditions of a bipolar junction transistor.

From left: John Bardeen, William Shockley and Walter Brattain who worked in the Bell Laboratories in New Jersey, America, which is the research arm of the company American Telephone and Telegraph (AT&T). Shockley worked for ten years on the physics of the transistor but it was John Bardeen and William Brattain who created the “point contact transistor” under his supervision. However, the "bipolar" transistor, which was superior to the point contact transistor, was designed by Shockley. So, we can say that the bipolar junction transistor was largely Shockley's creation. The bipolar junction transistor was successfully demonstrated at the Bell Labs and its discovery was announced in a press release on July 4, 1951. Shockley, Bardeen and Brattain were jointly awarded the Nobel Prize in Physics in 1956.

## 3.2.1 Construction

Let us begin the discussion by asking: **What is a bipolar junction transistor (BJT)**? How is it constructed?

A bipolar junction transistor is a three-terminal device as shown in Fig. 3.1a. It is constructed by doping a single crystalline semiconducting material (usually silicon or germanium) in two ways:

i) by sandwiching a thin layer of *p*-type semiconductor between two outer layers of *n*-type semiconductor forming an *n*-*p*-*n* transistor; or

ii) by sandwiching a thin layer of *n*-type semiconductor between two outer layers of *p*-type semiconductor forming a *p*-*n*-*p* transistor.

This kind of doping makes it possible to use a BJT as an amplifier or a switch (see Fig. 3.1b).

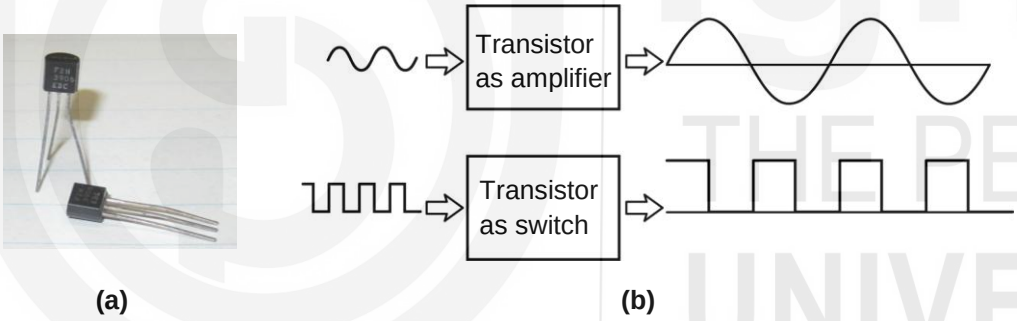



**Fig. 3.1**: **a) A bipolar junction transistor is a three-terminal device, which can be used b) as an amplifier and a switch.**

So, in a bipolar junction transistor, there are **three regions doped alternately** by *n*-type and *p*-type impurities to create an *n*-*p*-*n* or a *p*-*n*-*p* type of structure. Fig. 3.2 shows the structure of an *n*-*p*-*n* transistor.

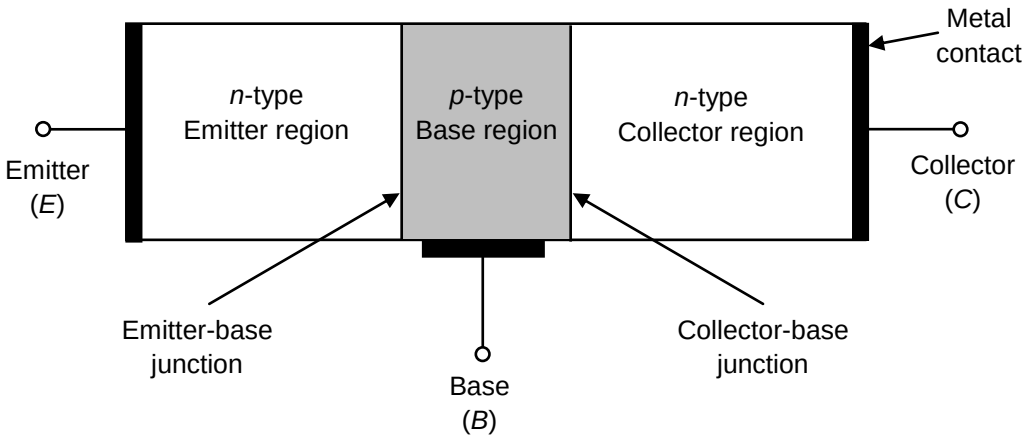



**Fig. 3.2**: **Structure of an *n*-*p*-*n* transistor.**

The three regions (*n*, *p* and *n*) shown in Fig. 3.2 are called **emitter** (*E*), **base** (*B*) and **collector** (*C*), respectively. So, the BJT is a **three-terminal device** with the electrical contact terminals attached to the emitter, base and collector. Sometimes, this is indicated by the letters E, B and C marked on the transistor.

The emitter, base and collector regions in a transistor are doped differently and have different widths. The emitter is doped heavily because its role is to 'emit' or inject charge carriers into the base region. The base region is lightly doped and is made very thin so that the heat loss due to recombination of charge carriers in it is reduced. The collector's doping levels lie between those of the emitter and the base. The collector is the largest of the three regions because it collects the charge carriers and has to dissipate more heat than the emitter or base. As you can see in Fig. 3.2, the transistor has two *p*-*n* junctions – one *p*-*n* junction is between the emitter and the base and the other *p*-*n* junction is between the base and the collector:

- **Emitter-base junction**, and
- **Collector-base junction**.

That is why a bipolar junction transistor can be thought of as having two *p*-*n* junctions back-to-back: one **emitter-base junction** and the other **collector-base junction**.

You may like to fix the structure of a BJT in your mind before you learn about its working. Try SAQ 1.

---

### *SAQ 1* – Bipolar junction transistor structure

a) Draw a labelled diagram showing the structure of a *p*-*n*-*p* transistor in the manner shown in Fig. 3.2 for an *n*-*p*-*n* transistor.

b) List the emitter, base, collector regions in a BJT in the order of (i) increasing levels of doping; (ii) increasing width.

---

## 3.2.2 Biasing and Working Mechanism

You can think of the *n*-*p*-*n* transistor as an *n*-*p* junction followed by a *p*-*n* junction. And the *p*-*n*-*p* transistor as a *p*-*n* junction followed by an *n*-*p* junction. So, we can understand its working in terms of the working of the two back-to-back *p*-*n* junctions.

Since there are two *p*-*n* junctions in a BJT, there will be **two depletion regions in the transistor** when no voltage is applied across the transistor due to diffusion of free electrons across the emitter-base and collector-base junctions. But **these will not be of the same width**. Can you say, why? This is because of the **different doping levels** of the emitter, base and collector.

Since the emitter is heavily doped, there will be a greater concentration of ions near the emitter-base junction preventing movement of charges across the junction. This will result in a thin depletion layer. Since the base region is

lightly doped, it will have a wider depletion region as the concentration of ions on that side of the junction is less. So, the depletion region will be of lesser width in the emitter region as compared to the base region. This means the depletion layer extends well into the base and only slightly into the emitter (see Fig. 3.3).

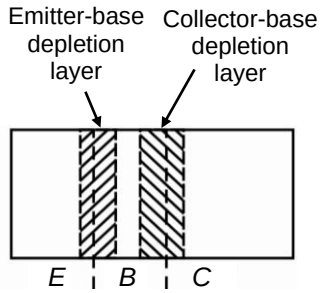



**Fig. 3.3**: **Depletion layers in a transistor when no voltage is applied.**

Similarly, at the collector-base junction, the depletion region in the base region is wider than that in the collector region. Since the collector is doped lesser as compared to the emitter, the collector-base depletion layer is wider than the emitter-base depletion layer (Fig. 3.3).

For each depletion layer, the barrier potential is about 0.7 V at 25°C for a silicon transistor and 0.3 V for a germanium transistor. Do you know that silicon transistors are more widely used than germanium transistors because of higher voltage rating, greater current ratings, and low temperature sensitivity? For our discussion, we will refer to silicon transistors, unless indicated otherwise.

In order that a transistor functions properly, we need to apply suitable voltages to its terminals. This is called the **biasing** of the transistor. So, the working of a bipolar junction transistor depends on the way the two *p*-*n* junctions in the transistor are biased. We take the case of an *n*-*p*-*n* transistor to explain transistor biasing and working mechanism. In our discussion, we consider an *n*-*p*-*n* transistor because it is more commonly used.

A typical biasing scheme of an *n*-*p*-*n* transistor is shown in Fig. 3.4. Note from Fig. 3.4 that in an *n*-*p*-*n* transistor, the **emitter-base** *p*-*n* **junction is forward biased while the collector-base** *p*-*n* **junction is reverse biased** for its normal operation as an amplifier.

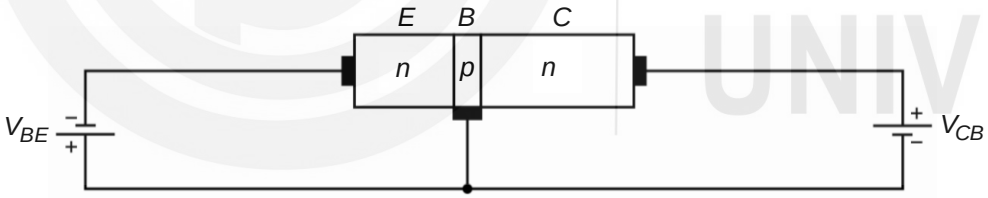



**Fig. 3.4**: **An** *n*-*p*-*n* **transistor when the emitter-base junction is forward biased and collector-base junction is reverse biased.**

We now ask: **What happens when we forward bias the emitter-base junction and reverse bias the collector-base junction** in a transistor? Refer to Figs. 3.5a, b and c. Note that the base (*p*-type) is biased positively with respect to the emitter (*n*-type). So, what will happen in this kind of biasing?

Note that there are free electrons in the emitter region (Fig. 3.5a). When the applied voltage $V_{BE}$ is greater than the barrier potential (0.6 to 0.7 V for silicon transistor), these electrons enter the base region (see Fig. 3.5b). Once inside the base, these electrons can flow either through the thin base into the external base lead, or across the collector junction into the collector region. Since the base region is very thin and it receives a large number of electrons, therefore, for $V_{BE} > 0.7\,\text{V}$, most of these electrons diffuse into the collector depletion layer.

The free electrons in this layer are pushed into the collector region (by the depletion layer field and the positive voltage $V_{CB}$ applied to the collector terminal) as shown in Fig. 3.5c, and flow into the external collector lead.

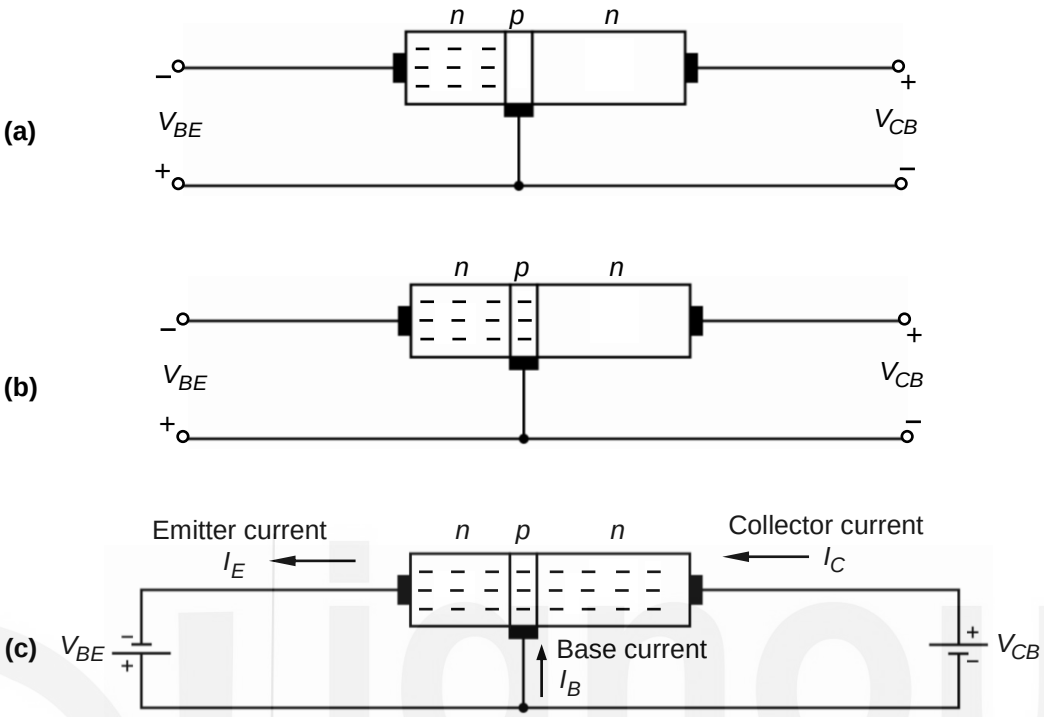



**Fig. 3.5**: **In an *n-p-n* transistor with forward-biased emitter and reverse-biased collector, a) emitter has many free electrons; b) free electrons are injected into base; c) free electrons diffuse to collector through base.**

So, due to the extremely thin base region and the positive voltage applied to the collector, almost all electrons diffuse through the base to the collector (Fig. 3.5c). This results in **current flow into the collector**. This current is called the **collector current** and denoted by $I_C$. It is of the order of milliamperes in a typical transistor.

Now let us see if any current flows through the base. Since the base region is very thin, most of the electrons cross to the collector region. Only a very small number of electrons flow out of the base terminal.

So, the **base current** that **flows into the base terminal** is very small. It is denoted by $I_B$ and is of the order of microamperes. In most transistors, more than 95 percent emitter-injected electrons flow to the collector; less than 5 percent flow out in the external base lead.

The emitter current (denoted by $I_E$) is the current that flows **out of the emitter**. Typically, the emitter and collector currents are of the order of milliamperes and the base current is a few microamperes.

In sum, we can say that a steady stream of electrons leaves the negative source terminal and enters the emitter region. The forward bias forces these electrons to enter the base region. Almost all these electrons diffuse into the collector depletion layer, through the base due to the depletion layer field and the positively biased collector resulting in a steady stream of electrons into the collector region.

Fig. 3.6a shows the circuit symbol of an *n-p-n* transistor. The arrow shows the direction of current flow when the emitter-base *p-n* junction is biased in the forward direction, which means that the base is biased positively with respect to the emitter.

Similarly, the circuit symbol of a *p-n-p* transistor is shown in Fig. 3.6b.

You have learnt that the transistor has two *p-n* junctions, one of which is forward biased and the other reverse biased. Recall from Unit 2 that the forward biased *p-n* junction has low forward resistance and reverse biased *p-n* junction has high reverse resistance.

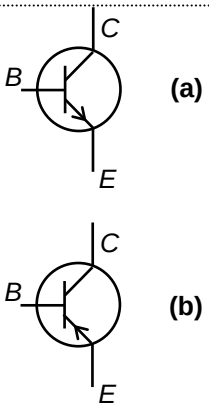



**Fig. 3.6**: **Circuit symbols of a)** *n-p-n* **transistor; b)** *p-n-p* **transistor.**

You should always remember that

> The emitter-base (*p-n*) junction in a transistor is forward biased and offers low forward resistance. The collector-base (*p-n*) junction in the transistor is reverse biased and, therefore, offers high reverse resistance.


This property of the transistor, of transferring a weak input signal from low resistance circuit to high resistance circuit, results in the input signal getting amplified in a particular configuration called the common emitter configuration (about which you will learn in Unit 4).

This happens because even if the collector current is in milliamperes, the **high reverse resistance** circuit results in an output signal having much larger amplitude than the input signal.

The transistor gets its name from what was historically referred to as *transresistance* : (*trans from transfer + istor from resistor*). Thus, transfer + resistor = transistor.

From this discussion, **you should not conclude that you can connect two discrete diodes back-to-back to get a transistor**.

This is because in such a circuit, each diode has two doped regions, and the overall circuit would have four doped regions. Also, the base region is not the same as in a transistor.

**The key to transistor action, therefore, is the lightly doped thin base between the heavily doped emitter and the intermediately doped collector. Free electrons passing through the base stay in the base for a short time and reach the collector**.

Effectively, the base current controls the BJT operation and it is a **current-controlled device**.

Let us now write down the relationship between the emitter, base and collector currents. Applying Kirchhoff's current law to the transistor as if it were a single node, we get:

$$I_E = I_B + I_C \qquad (3.1a)$$

Since $I_B << I_C$, we can write:

$$I_E \approx I_C \qquad (3.1b)$$

Always remember the sign convention for the currents in a BJT given ahead.


Recall that the convention for current direction is that the direction of current flow is taken to be opposite to that of the direction of electron flow. The emitter, base and collector **currents are taken to be positive** when these flow **into** the transistor. For the *n*-*p*-*n* transistor, the emitter current is negative and the collector and base currents are positive. For the *p*-*n*-*p* transistor, the emitter current is positive and the collector and base currents are negative.

Now, before we move on to the next section on the field effect transistor, you may like to revise the biasing and working of a bipolar junction transistor. Attempt SAQ 2.

### *SAQ 2* – Bipolar junction transistor biasing and working

a) Draw a labelled diagram similar to Fig. 3.4 showing how a *p*-*n*-*p* transistor is biased.

b) State the magnitudes of the emitter, base and collector currents in the *p*-*n*-*p* transistor. The emitter current in a BJT is 5.0 mA and the collector current is 4.998 mA. What is the value of the base current in it?

## 3.3 FIELD EFFECT TRANSISTOR

In this section, you will learn about the construction, biasing and working mechanism of the field effect transistor or FET. The FET is also a double junction device but it is different from the BJT: Whereas in the bipolar junction transistor both majority and minority charge carriers flow, in an FET **only majority charge carriers (either electrons or holes, but not both) flow**. That is why it is called a **unipolar device**. (Remember that **BJT** is a **bipolar device** because the currents in it are due to both electrons and holes).

The first FET was built and patented by the German physicist Heinrich Welker in 1945. It was called the junction field-effect transistor (JFET) about which you will learn in this section. A working JFET was built by George F. Dacey and Ian M. Ross in the Bell Laboratories in 1953.

Field effect transistors are of two types:

- **Junction field effect transistor** (JFET)
- **Metal oxide semiconductor field effect transistor** (MOSFET)

We will focus on the construction, biasing and working mechanism of JFET in our discussion. This device may be entirely new for you. So read the next two sections carefully.

### 3.3.1 Construction

Like the BJT, the JFET is also a three-terminal semiconductor device. It is made up of either an *n*-type or a *p*-type silicon substrate. Imagine a substrate

or bar of *n*-type semiconductor as shown in Fig. 3.7a. Note that its lower end is labelled as **source** and upper end as **drain**. If we apply a voltage so that the drain is positive with respect to the source, electrons will flow from the source to the drain in the substrate.

Now refer to Fig. 3.7b. To create a JFET, the *n*-type substrate/bar of semiconductor is doped heavily with *p*-type material at two sides so that there are two *p*-*n* junctions at the sides of the JFET. The *p*-regions are connected internally so that there is a **single gate** lead. This kind of JFET is called the *n*-channel JFET. The majority charge carriers in it are electrons.

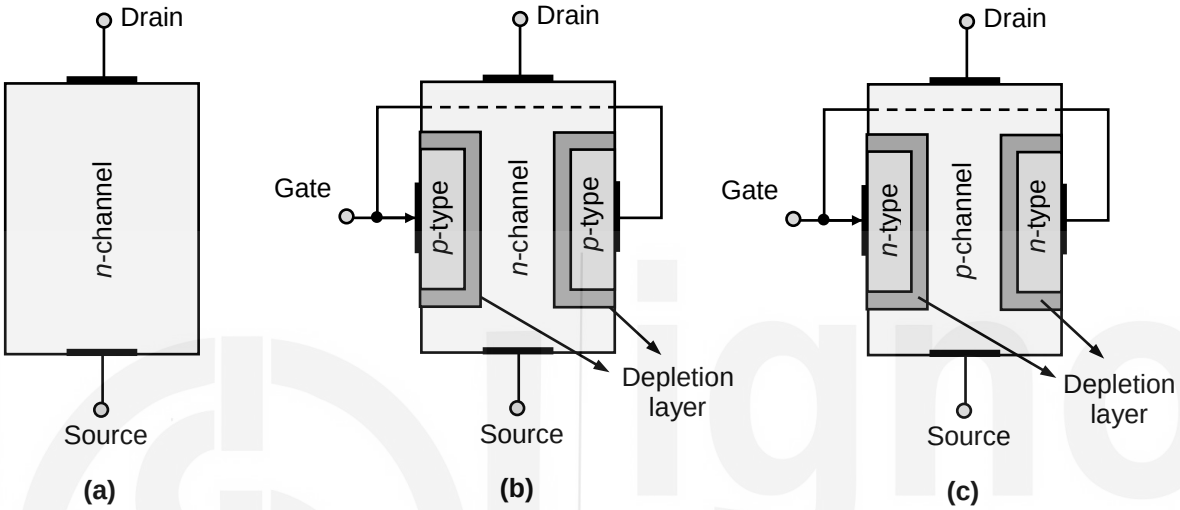



**Fig. 3.7**: **a) Drain and source in an *n*-channel JFET; b) its structure; c) a *p*-channel JFET.**

If the substrate or bar is of *p*-type material, then its sides are doped with *n*-type material and it is called a *p*-channel JFET (see Fig. 3.7c). Holes are majority charge carriers in it.

Just as we focused on the *n*-*p*-*n* transistor in Sec. 3.2, we will mainly discuss the *n*-channel JFET in this section. Then you can apply the ideas to *p*-channel JFET for practice and revision.

From Fig. 3.7b, note that the major part of the JFET is the *n*-channel. The top of the channel is connected through an ohmic contact to a terminal called the **drain** (*D*). The lower end of the channel is connected through another ohmic contact to a terminal called the **source** (*S*). The two *p*-type materials are connected to each other internally and externally to the third terminal called the **gate** (*G*).

So, always remember that

> In an *n*-channel JFET, the drain and source are connected to the two opposite ends of the *n*-channel and the gate to the two layers of the *p*-type material. The *n*-type material is heavily doped in the regions near the source and drain terminals.


You can see that like the BJT, the JFET is a three-terminal device (source, gate, drain) that has two *p*-*n* junctions. Thus, in an *n*-channel JFET,

**Source** *S* is the terminal of the JFET through which the majority carriers **enter** the channel giving rise to the source current $I_S$. Following the convention of the direction of current as opposite to the flow of electrons, we take the current flowing into the channel at *S* as positive.

**Drain** *D* is the terminal through which the majority carriers **leave** the channel giving rise to the drain current $I_D$. By convention, we take the current leaving the channel at *D* as positive.

**Gate** *G* is the term used for the terminal attached to the heavily doped (*p*+) regions on both sides of the *n*-type channel.

**Channel** is the region of *n*-type material between the two gate regions through which the majority carriers move from source to drain.

The drain-to-source voltage is denoted by $V_{DS}$ and in an *n*-channel JFET, *D* is positively biased with respect to *S*.

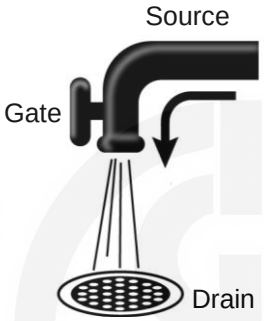



**Fig. 3.8**: **Analogy of water flow from water tap for the JFET.**

We can use an analogy to understand the role of these terminals in a simple way. Consider water flowing from a tap (Fig. 3.8). The source of water pressure is similar to the voltage applied between drain and source. Just as the water source establishes water flow from the tap, so does the voltage $V_{DS}$ establish a flow of electrons from the source. A potential applied at the gate controls the flow of electrons to the drain (just as water flow is controlled by turning the tap's handle). Water flows out of the drain as do electrons in the JFET. As in a tap, the drain and source terminals are at the opposite ends of the *n*-channel.

You may now like to revise the construction of a JFET. Solve SAQ 3.

---

### *SAQ 3* – JFET construction

a) What is the main difference between the construction of an *n*-channel JFET and a *p*-channel JFET?

b) Name the majority charge carriers in *n*-channel and *p*-channel JFETs.

c) Fill in the blanks in the following sentence:

In a *p*-channel JFET, the source is the terminal through which ……..enter the substrate and leave the channel through the terminal called the …… The gate refers to the heavily doped….-type material on both sides of the JFET.

---

Let us now describe the biasing and working of an *n*-channel JFET.

## 3.3.2 Biasing and Working Mechanism

In the absence of an applied voltage, there exist depletion regions at the two *p*-*n* junctions on the sides of the *n*-channel JFET. Since the *p*-type material is heavily doped, the depletion layer is thin in the *p*-region and extends into the *n*-region (see Figs. 3.7a and b).

We now ask: **How is the JFET biased for its normal functioning**?

Refer to Fig. 3.9, which shows an *n*-channel JFET. We first consider the case when a positive voltage ($V_{DS}$) is applied to the drain with respect to the source and the gate is connected directly to the source so that the voltage $V_{GS}$ between the gate and source is zero:

a) $V_{DS} > 0$ **and** $V_{GS} = 0$ V

In this case, the gate and the source are at the same potential and under no bias conditions when $V_{DS}$ is zero, the depletion layers at the *p*-*n* junctions will be as shown in Fig. 3.7a.

Now what happens when the drain is biased positively with respect to the source by a battery or power supply ($V_{DD}$)? Electrons in the *n*-channel move towards the drain since it is positively biased. This results in the flow of drain current in the direction shown in Fig. 3.9. The flow of electrons is unhindered in the channel and hence, the source current is equal to the drain current when $V_{GS}$ is zero.

**REMEMBER:** The polarity of the drain-source voltage will be reversed for a *p*-channel JFET and so will the directions of the drain and source currents but the underlying physics remains the same.

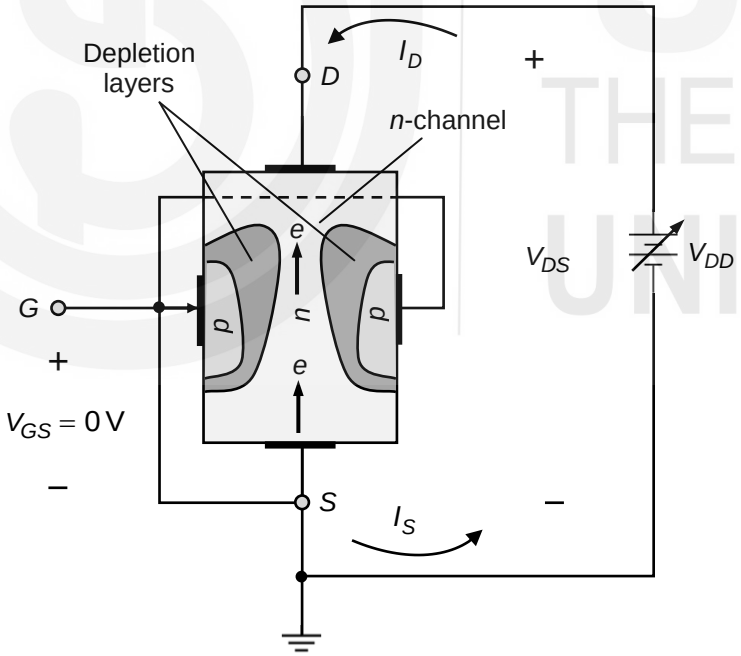



**Fig. 3.9**: **Working of JFET when** $V_{DS} > 0$ **and** $V_{GS} = 0$ V**.**

Also note from Fig. 3.9 that the *p*-*n* junctions are reverse biased in this case. You can see that the *p*-regions are negatively biased with respect to the *n*-region near the drain because the gate terminal is connected to the source terminal, which is negatively biased with respect to the drain. So, virtually no electrons move to the gate and the gate current is zero. Thus, we have:

$$I_D = I_S \qquad (3.2a)$$

and $I_G = 0$ (3.2b)

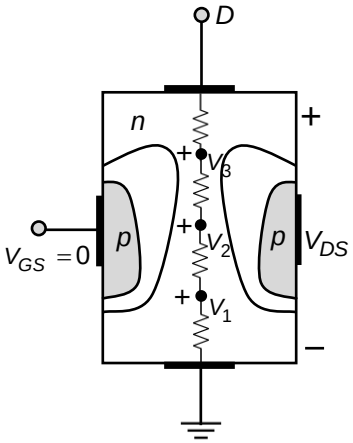



**Fig. 3.10**: **Variation in reverse biasing voltages across the *p-n* junctions; $V_3 > V_2 > V_1$ and $V_{GS} = 0$ V.**

Now did you note in Fig. 3.9 that the depletion layers of the *p-n* junctions are wider towards the drain end as compared to the source end? You may like to know: **Why is it so**?

This is because of the resistance of the channel. Let us assume that the resistance of the channel is uniform. Then we can break it down into segments of resistances as shown in Fig. 3.10. The voltage applied between the drain and the source drops across these resistances, and we have maximum voltage at the drain and minimum at the source.

As a result, the upper ends (towards the drain end of the channel) of both *p-n* junctions will be more reverse biased compared to their lower ends (towards the source end of the channel). In fact, the reverse bias between the *p*-type gate and *n*-type channel is **zero near the source end** and **maximum near the drain end**. Recall from Unit 2 that the greater the reverse bias in a *p-n* junction, the wider will be the depletion layer.

Therefore, **the depletion layers are much wider near the drain end and extend more into the channel in comparison with the source end**. This is how we get the **wedge shape of the *n*-channel** shown in Fig. 3.9.

Now what happens when we increase $V_{DS}$ ? The drain current will increase in accordance with Ohm's law. Fig. 3.11 shows the drain characteristics of a JFET, the plot of the drain current $(I_D)$ and drain-source voltage $(V_{DS})$ for $V_{GS} = 0$. Note that when $V_{DS}$ is gradually increased, in the initial stages, the curve is linear. This is because the resistance is constant in this ohmic region.

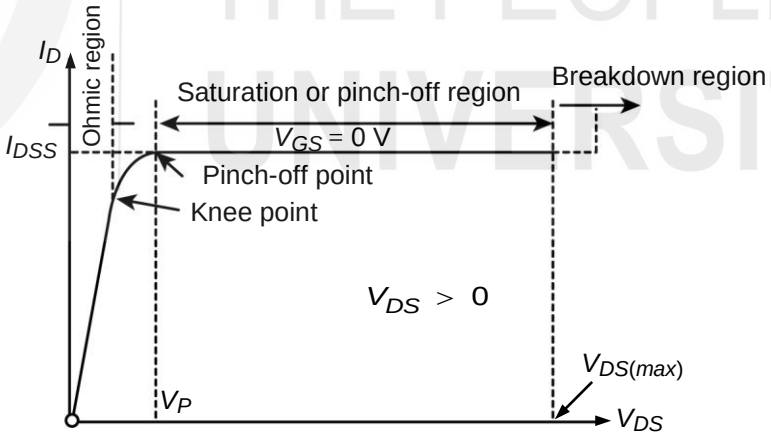



**Fig. 3.11**: **Drain characteristics of JFET when $V_{DS} > 0$ and $V_{GS} = 0$ V.**

As $V_{DS}$ is increased further, the depletion layers become wider and the channel width reduces. The reduced width decreases the path of conduction for electrons, causing the resistance of the channel to increase. Then the curve begins to level off and eventually the drain current $I_D$ saturates. After that it does not increase any further with an increase in $V_{DS}$. The drain-source voltage at which the drain current saturates is called the **pinch-off voltage** and denoted by $V_P$. So, $I_D$ saturates for $V_{DS} \geq V_P$. This happens when $V_{DS}$ is increased to a value such that the two depletion layers "touch" each other as shown in Fig. 3.12 resulting in *pinch-off*.

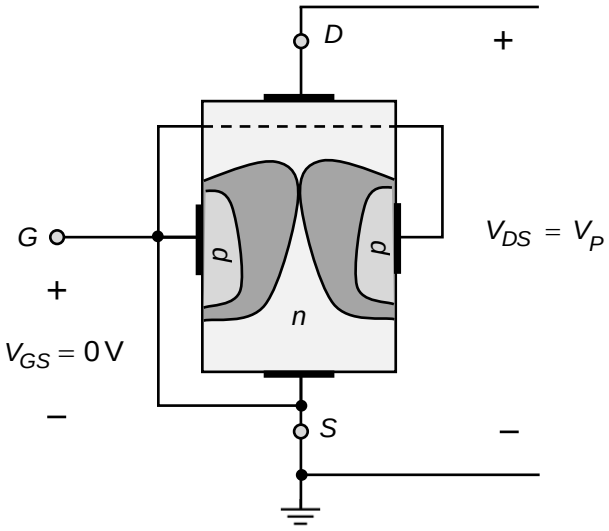



**Fig. 3.12**: **Pinch-off in JFET;** $V_{DS} = V_P$ **and** $V_{GS} = 0$ V**.**

**Do not misunderstand the term pinch-off. It does NOT mean that the drain current is "pinched off". That is, the drain current does not become zero**!

Actually, the drain current becomes constant (saturates) and is denoted by $I_{DSS}$ as shown in Fig. 3.11. What happens is that a very small channel does exist and the saturation current flows through it. The notation $I_{DSS}$ is used for **the saturation current when the gate and the source are short-circuited**. So, always remember that

> $I_{DSS}$ **is defined by the conditions** $V_{DS} \geq |V_P|$ **and** $V_{GS} = 0$ **and is the maximum drain current in a JFET.**


You may like to know: **Why does the drain current not become zero at the pinch-off voltage**? It is because even if the depletion layers from both sides are touching, there is always some narrow channel allowing the drift current to pass through.

Thus, when $V_{DS}$ becomes greater than $V_P$, the drain current becomes constant and remains at the same level. In effect, the JFET becomes a current source for $V_{DS} \geq V_P$ (Fig. 3.13).

Note from Fig. 3.13 that the drain saturation current $I_{DSS}$ is constant but the voltage $V_{DS}$ $(> V_P)$ is determined by the load in the circuit.

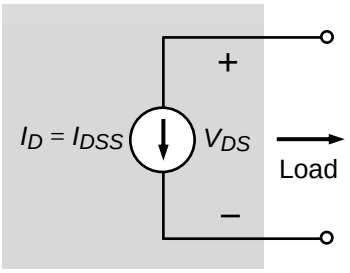



**Fig. 3.13: Current source equivalent of JFET when** $V_{DS} > V_P$ **and** $V_{GS} = 0$ V**.**

Let us now ask: **What kind of drain characteristics do we obtain when the gate source voltage** $V_{GS}$ **is non-zero**?

So, we consider the case when a **negative voltage is applied to the gate** of an *n*-channel JFET.

b) $V_{DS} > 0$ **and** $V_{GS} < 0$ V

Refer to Fig. 3.14. Note from the figure that the voltage from gate to source is negative, that is, the gate is negatively biased with respect to the source. Thus, the gate-source *p*-*n* junctions are reverse biased by $V_{GS}$. So, if the

input signal is applied to the gate terminal, it will experience a high resistance. In other words, the JFET will offer high input impedance to the input signal. (It is always beneficial to have high input impedance so that the current drawn from the signal source is very small, and hence, there are no loading effects.) Also, the depletion layers will be wider due to the reverse biased gate junction as compared to the case when $V_{GS}$ is zero (case a).

Now if we apply $V_{DS}$, pinch-off will occur at a lower value of voltage $V_{DS}$ because depletion layer widths for pinch-off will now be reached at a **lower value** of $V_{DS}$. The gate current $I_G$ will be zero in this case too because $V_{GS}$ is negative and electrons will not flow through the gate.

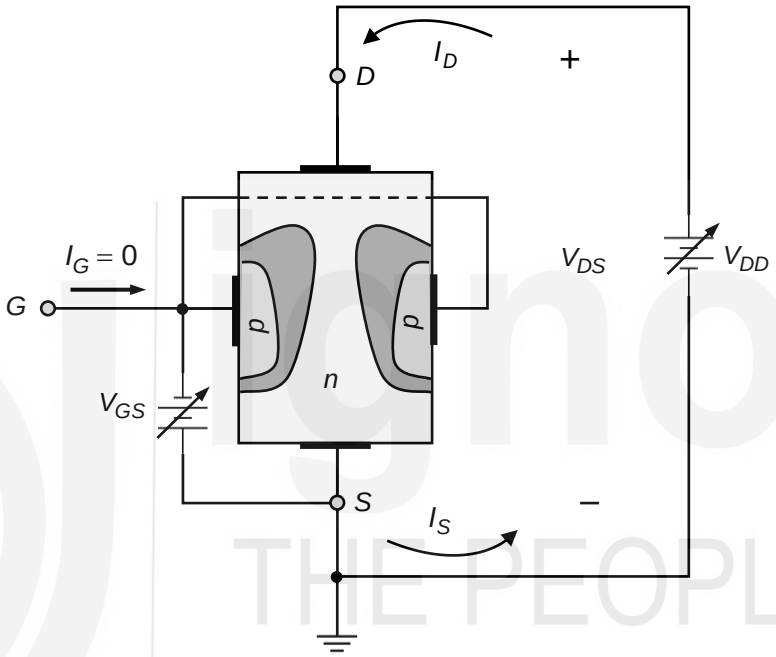



**Fig. 3.14**: **Working of JFET when $V_{DS} > 0$ and $V_{GS} < 0$.**

Therefore, the effect of applying a negative bias to the gate is that the drain current will reach its saturation level for a lower value of $V_{DS}$. Also, the saturation level value of the drain current ($I_{DSS}$) will decrease. Fig. 3.15 shows the drain (*I*-*V*) characteristics of an *n*-channel JFET.

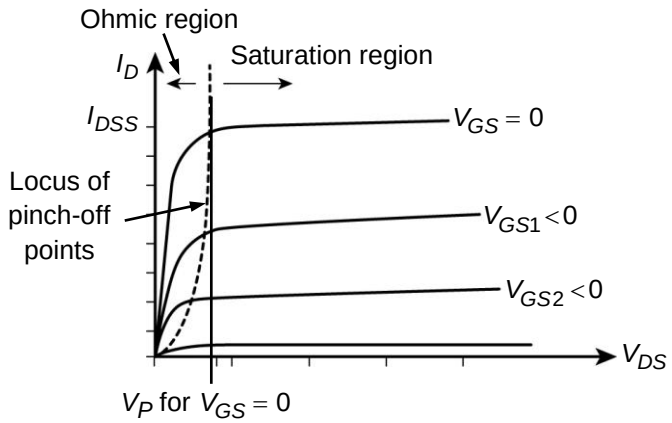


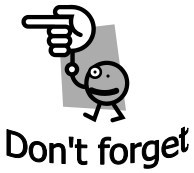

**Fig. 3.15**: **Drain characteristics of an *n*-channel JFET when $V_{DS} > 0$ for different values of $V_{GS} \leq 0$.**

Note from the figure that as the voltage $V_{GS}$ is made more and more negative, saturation of the drain current occurs at lower values of $V_{DS}$. When $V_{GS}$ reaches the pinch-off voltage, that is, $V_{GS} = -V_P$, the saturation current becomes zero for all practical purposes. At that point, the JFET is "turned off".

Always remember,

**The gate-source voltage controls current flow in the JFET**.

**The voltage $V_{GS} = V_P$ is that value of $V_{GS}$ for which the drain current is zero ($I_D = 0$). The voltage $V_P$ is <u>negative</u> for an *n*-channel JFET and <u>positive</u> for a *p*-channel JFET.**




For very high values of $V_{DS}$, these curves suddenly become almost vertical (see Fig. 3.11). The vertical rise in current indicates breakdown of the JFET. The operation of JFET at such high voltage has to be avoided to prevent damaging it.

The circuit symbol of an *n*-channel JFET is shown in Fig. 3.16. **Remember that the direction of the arrow represents the direction in which the gate current would flow if the *p*-*n* junction were forward biased**.

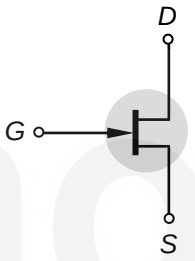



**Fig. 3.16**: **Circuit symbol of an *n*-channel JFET.**

With this, we end the discussion on JFET. You should try SAQ 4 to check whether you have understood the biasing and working of a JFET.

## *SAQ 4* – JFET biasing and working

a) Draw the circuit diagram analogous to Fig. 3.9 for a *p*-channel JFET for $V_{GS} = 0$ V.

b) Draw the circuit symbol of a *p*-channel JFET.

In this section, you have learnt about one type of a field effect transistor, namely, the JFET. We have not discussed the MOSFET about which you will learn in higher classes.

You have learnt that in the junction field effect transistor, the output current, i.e., the drain current between the drain and the source is controlled by the gate-to-source voltage $V_{GS}$, the input voltage applied at the gate with reference to the source.

So, a field-effect transistor **uses an electric field** to control the flow of current in a semiconductor. That is where the name field effect transistor comes from. And that is why a JFET is a **voltage-controlled device**.

You have learnt that the value of $V_{GS}$ determines how much drain current flows in a JFET. When $V_{GS} = 0$, the saturation drain current $I_{DSS}$ flowing through the JFET is maximum. This is why a JFET is referred to as **a normally on** device.

If $V_{GS} = |V_P|$, ($-V_P$ for *n*-channel JFET and $+V_P$ for *p*-channel JFET), the depletion layers touch and the drain current is cut off. Then the JFET is turned off.

We now summarise what you have learnt in this unit.

## 3.4 SUMMARY

| Concept | Description |
|---|---|
| ***Bipolar junction transistor and its construction*** | ■ A bipolar junction transistor is a double junction three-terminal device. It is constructed by doping a single crystalline semiconducting material (usually silicon or germanium) in two ways:<br>• by sandwiching a thin layer of *p*-type semiconductor between two outer layers of *n*-type semiconductor forming an *n*-*p*-*n* transistor; or<br>• by sandwiching a thin layer of *n*-type semiconductor between two outer layers of *p*-type semiconductor forming a *p*-*n*-*p* transistor.<br>This kind of doping makes it possible to use a BJT as an amplifier or a switch. Both electrons and holes give rise to the current in a BJT. Hence, it is given the name bipolar.<br>The three regions in an *n*-*p*-*n* transistor (*n*, *p* and *n*) or a *p*-*n*-*p* transistor (*p*, *n* and *p*) are called **emitter** (*E*), **base** (*B*) and **collector** (*C*), respectively. |
| ***Biasing and working of BJT*** | ■ Transistor action in a BJT occurs because of the different doping levels of the emitter, base and collector regions, their different widths and the way it is biased.<br>• The base is lightly doped and is very thin compared to the emitter and collector regions. The emitter region is more heavily doped compared to the collector region.<br>• Typically, in a transistor used as an amplifier, the emitter-base junction is forward biased and the collector-base junction is reverse biased.<br>• The emitter current is large (in milliamperes) and the base current is very small (in microamperes or nanoamperes) so that the collector current is almost equal to the emitter current:<br>$I_E = I_B + I_C$<br>Since $I_B << I_C$, we can write:<br>$I_E \approx I_C$<br>• The BJT is a current-controlled device as its operation is controlled by the currents in it. |
| ***Junction field effect transistor*** | ■ The field effect transistor is also a double junction three-terminal device that has two *p*-*n* junctions. An *n*-channel JFET is constructed by heavily doping the sides of an *n*-type substrate with *p*-type material so that there are two |

*p*-*n* junctions at the sides of the JFET. A *p*-channel JFET is constructed by heavily doping the sides of a *p*-type substrate with *n*-type material. JFETs have only one type of charge carriers for current flow and that is why these are unipolar devices. Electrons are the majority charge carriers in an *n*-channel JFET and holes in a *p*-channel JFET.

The three terminals are called the source (*S*), gate (*G*) and drain (*D*) analogous to the emitter, base and collector in a BJT. The gate regions are heavily doped as compared to the channel. So, the depletion layer extends more in the channel than in the gate regions.

***Biasing and working of JFET***

- For its normal functioning, an *n*-channel JFET is biased so that its drain is positive with respect to the source, and the gate-source voltage is zero or negative.

Thus, when $V_{DS} > 0$ and $V_{GS} = 0$ V, electrons in the *n*-channel move from the source towards the drain resulting in the drain current into the JFET. The source current is equal to the drain current when $V_{GS}$ is zero:

$$I_D = I_S \quad \text{and} \quad I_G = 0$$

- When $V_{DS} > 0$, the depletion layers of the *p*-*n* junctions are much wider near the drain end and extend more into the channel in comparison with the source end, resulting in a **wedge-shaped** *n*-channel.
- When $V_{DS}$ is relatively low, the drain current increases in accordance with Ohm's law and the drain current versus the drain-source voltage curve is linear.
- As $V_{DS}$ is increased further, the depletion layer widths increase due to which the channel width decreases causing increased impedance to the flow of drain current. This results in saturation of the drain current, which does not increase with any further increase in $V_{DS}$.
- The drain-source voltage at which the drain current saturates is called the **pinch-off voltage** $V_P$.
- Pinch-off in a JFET occurs when $V_{DS}$ is increased to a value such that the two depletion layers "touch" each other.
- $I_{DSS}$ is defined by the conditions $V_{DS} \geq |V_P|$ and $V_{GS} = 0$ and is the maximum drain current in any JFET.
- When $V_{DS} > 0$ and $V_{GS} < 0$, the drain current reaches its saturation level for a lower value of $V_{DS}$ and its value decreases.
- As the voltage $V_{GS}$ is made more and more negative, saturation of the drain current occurs at lower values of $V_{DS}$.
- When $V_{GS} = -V_P$, the saturation current becomes zero and at that point, the JFET is "turned off".
- At very high values of $V_{DS}$, breakdown occurs in a JFET.

## 3.5 TERMINAL QUESTIONS

1. Fill in the blanks in the following sentences:

   a) The BJT and JFET have ……*p*-*n* junctions. That is why these are called……..junction devices.

   b) A BJT is a ……..controlled device while a JFET is a……controlled device.

   c) The …… and the ……. control the flow of current in the BJT and JFET, respectively.

   d) In the BJT, current flow is due to ……while in a JFET, current flow is due to ……

   e) In a BJT, the ……..junction is forward biased and the ……junction is reverse biased; in a JFET, the ……. junction is reverse biased.

2. a) Name the majority and minority charge carriers in *p*-*n*-*p* and *n*-*p*-*n* transistors and explain which currents these constitute in them.

   b) What is meant by bipolar and unipolar devices?

3. Draw a *p*-*n*-*p* transistor biased for amplifier operation and label the currents that flow in it. Explain its working.

4. Can collector current be larger than emitter current in a BJT? Explain.

5. Write the main differences in the working mechanisms of the *p*-*n*-*p* and *n*-*p*-*n* transistors.

6. Why is JFET called a field effect transistor?

7. Explain pinch-off in a *p*-channel JFET with the help of a diagram.

8. Draw the labelled drain characteristics of a *p*-channel JFET showing the ohmic, saturation and breakdown regions. What is the value of the drain current when $V_{GS} = V_P$ in a *p*-channel JFET? When is the drain current in it maximum?

9. Explain why the JFET is termed a voltage-controlled device.

10. When a *p*-channel JFET is “turned off”, what happens to the saturation current in it? When the gate voltage becomes more negative in an *n*-channel JFET, what happens to the channel between the depletion layers?

## 3.6 SOLUTIONS AND ANSWERS

### Self-Assessment Questions

1. a) Fig. 3.17 shows the labelled diagram of the structure of the *p*-*n*-*p* transistor.

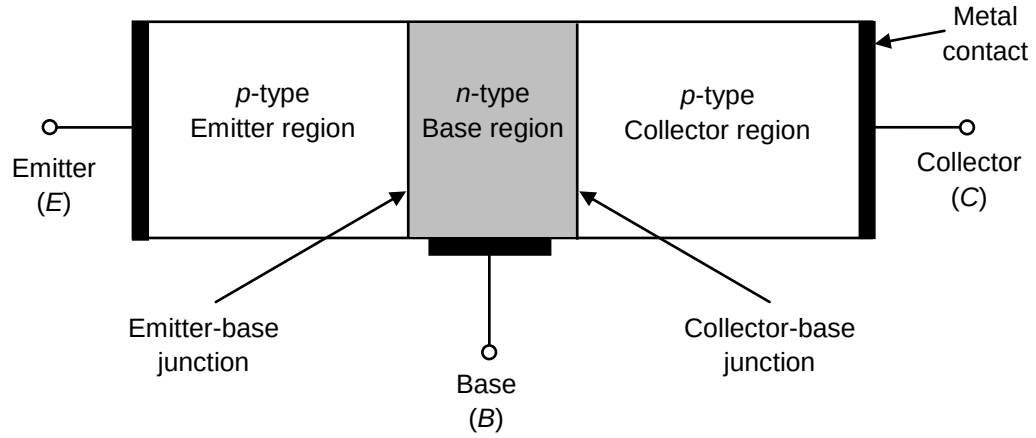



**Fig. 3.17**: **Structure of a *p-n-p* transistor.**

b) (i) increasing levels of doping: base, collector, emitter;

(ii) increasing width: base, emitter, collector.

2. a) Fig. 3.18 shows the labelled diagram of the biasing of the *p-n-p* transistor.

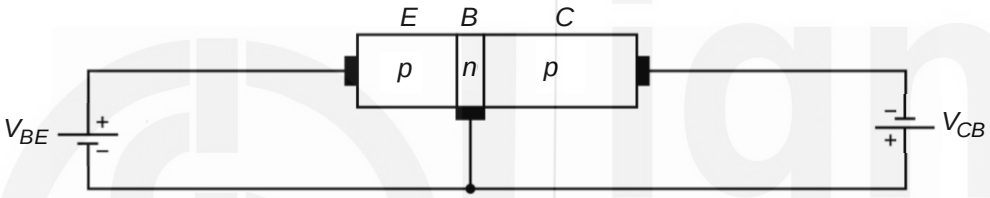



**Fig. 3.18**: **A *p-n-p* transistor when the emitter-base junction is forward biased and collector-base junction is reverse biased.**

b) The magnitudes of the emitter, base and collector currents in the *p-n-p* transistor are the same as those in an *n-p-n* transistor, that is, the emitter and collector currents are in milliamperes and the base current is in microamperes or nanoamperes. The base current is given from Eq. (3.1a) as:

$$I_B = I_E - I_C = 5.0\,\text{mA} - 4.998\,\text{mA} = 0.002\,\text{mA} = 2.0\,\mu A$$

3. a) In the *n*-channel JFET, the substrate/bar is made of *n*-type semiconductor and its sides are doped by *p*-type semiconductors. But in a *p*-channel JFET, the substrate/bar is made of *p*-type semiconductor and its sides are doped by *n*-type semiconductors.

b) The majority charge carriers in *n*-channel and *p*-channel JFETs are electrons and holes, respectively.

c) In a *p*-channel JFET, the source is the terminal through which holes enter the substrate and leave the channel through the terminal called the drain. The gate refers to the heavily doped *n*-type material on both sides of the JFET.

4. a) The circuit diagram analogous to Fig. 3.9 for the *p*-channel JFET when $V_{GS} = 0$ V is shown in Fig. 3.19.

b) The circuit symbol of a *p*-channel JFET is shown in Fig. 3.20.

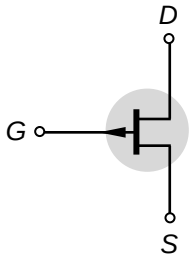



**Fig. 3.20**: **Circuit symbol of a *p*-channel JFET.**

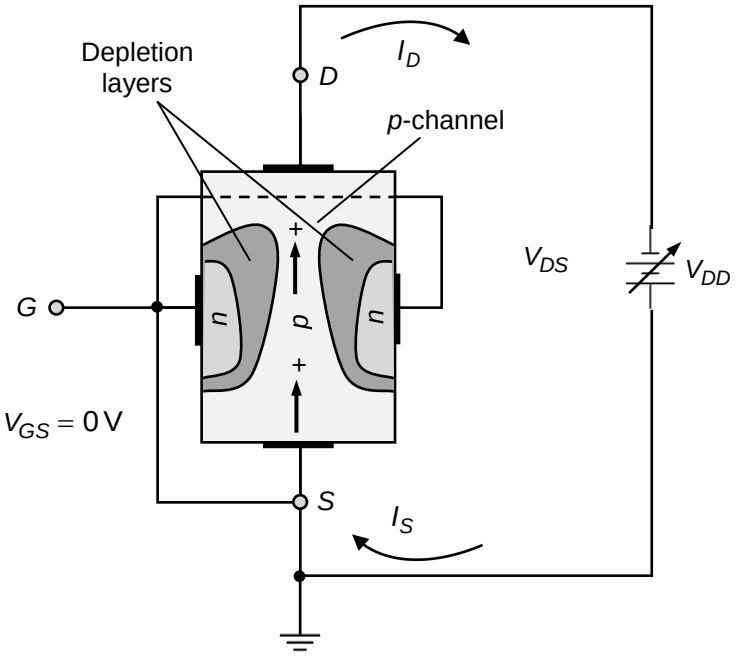



**Fig. 3.19**: **Circuit diagram for *p*-channel JFET when $V_{GS} = 0$ V.**

## Terminal Questions

1. a) The BJT and JFET have two *p*-*n* junctions. That is why these are called double junction devices.
   b) A BJT is a current-controlled device while a JFET is a voltage-controlled device.
   c) The base and the gate control the flow of current in the BJT and JFET, respectively.
   d) In the BJT, current flow is due to both majority and minority charge carriers (electrons and holes) while in a JFET, current flow is due to only majority charge carriers (electrons or holes).
   e) In a BJT, the emitter-base junction is forward biased and the collector-base junction is reverse biased; in a JFET, the gate-source junction is reverse biased.

2. a) In a *p*-*n*-*p* transistor, the majority and minority charge carriers are holes and electrons, respectively. The emitter and collector currents are due to the motion of holes, and the base current is due to the flow of electrons. In an *n*-*p*-*n* transistor, the majority and minority charge carriers are electrons and holes, respectively. The emitter and collector currents are due to the flow of electrons, and the base current is due to the motion of holes.
   b) In bipolar devices, current flow is due to both majority and minority charge carriers. In unipolar devices, current flow is due to only majority charge carriers.

3. Fig. 3.21 shows a *p*-*n*-*p* transistor biased for amplifier operation along with the currents that flow in it. Its working is analogous to that of an *n*-*p*-*n* transistor and is described below. Note from Fig. 3.21 that in a *p*-*n*-*p* transistor too, the emitter-base *p*-*n* junction is forward biased while the collector-base *p*-*n* junction is reverse biased for its normal operation as an amplifier.

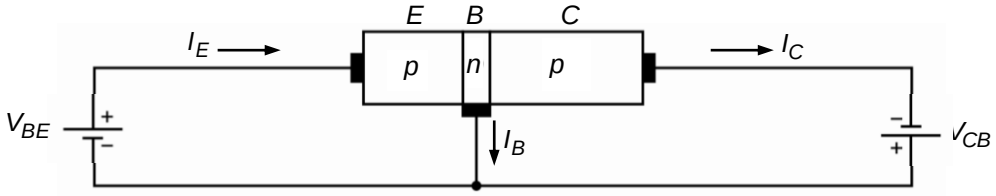



**Fig. 3.21**: **A *p*-*n*-*p* transistor biased for amplifier operation with its emitter-base junction forward biased and collector-base junction reverse biased.**

When the emitter (*p*-type) is biased positively with respect to the base (*n*-type), the holes in the emitter region enter the base region when the applied voltage $V_{BE}$ becomes greater than the barrier potential. Once inside the base, the holes can flow either through the thin base into the external base lead, or across the collector junction into the collector region. Since the base region is very thin and it receives a large number of holes, therefore, most of these holes diffuse into the collector depletion layer. The free holes in this layer are pushed into the collector region (by the depletion layer field and the negative voltage $V_{CB}$ applied to the collector terminal) and flow out of the collector. Due to the extremely thin base region and the negative voltage applied to the collector, almost all holes diffuse through the base to the collector. This results in current flow out of the collector. Since the base region is very thin, most of the holes cross to the collector region. Only a very small number of holes flow out of the base terminal. Therefore, the base current that flows out of the base terminal is very small. The emitter current flows into the emitter. Typically, the emitter and collector currents are of the order of milliamperes and the base current is a few microamperes.

4. No, the collector current cannot be larger than the emitter current in a BJT since a very small number of majority charge carriers from the emitter do flow out of (or into) the base of the BJT. Thus, the emitter current is the sum of the base current and the collector current.

5. The main differences in the working mechanisms of the *p*-*n*-*p* and *n*-*p*-*n* transistors are in their charge carriers and biasing, and the directions of the resulting currents. In an *n*-*p*-*n* transistor, the majority charge carriers are electrons, the *p*-type base is biased positively with respect to the *n*-type emitter, and the *n*-type collector is biased positively with respect to the *p*-type base. The emitter current flows out of the emitter, the base and collector currents flow into the base and collector regions, respectively. In a *p*-*n*-*p* transistor, the majority charge carriers are holes, the *n*-type base is biased negatively with respect to the *p*-type emitter, and the *p*-type collector is biased negatively with respect to the *n*-type base. The emitter current flows into the emitter, the base and collector currents flow out of the base and collector regions, respectively.

6. In a field effect transistor, the output current, i.e., the drain current between the drain and the source is controlled by the gate-to-source voltage $V_{GS}$, the input voltage applied at the gate with reference to the source. So, it uses an electric field to control the flow of current in a semiconductor. That is why the JFET is called a field effect transistor.

7. Fig. 3.22 shows the pinch-off in a *p*-channel JFET.

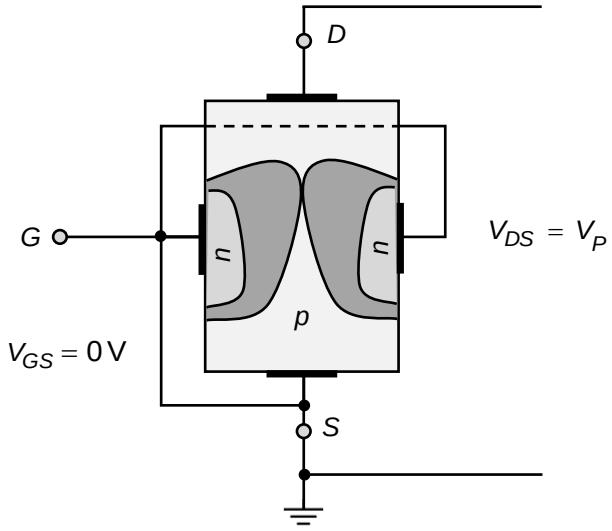



**Fig. 3.22**: **Pinch-off in *p*-channel JFET; $V_{DS} = V_P$ and $V_{GS} = 0$ V.**

Just as in an *n*-channel JFET, when $V_{DS}$ is increased in a *p*-channel JFET, the reverse bias across the gate-source *p*-*n* junction increases and the widths of the depletion layers increase resulting in a reduced channel width. This decreases the path of conduction for holes, causing the resistance of the channel to increase. Eventually the drain current $I_D$ saturates. After that it does not increase any further with an increase in $V_{DS}$. So when $V_{DS}$ is increased to a value $V_P$ such that the two depletion layers "touch" each other as shown in Fig. 3.22, pinch-off occurs in a *p*-channel JFET.

8. The drain characteristic curve for a *p*-channel JFET is shown in Fig. 3.23. The drain current in a *p*-channel JFET is zero when $V_{GS} = V_P$. It is maximum in a *p*-channel JFET when $V_{GS} = 0$ and $V_{DS} = V_P$.

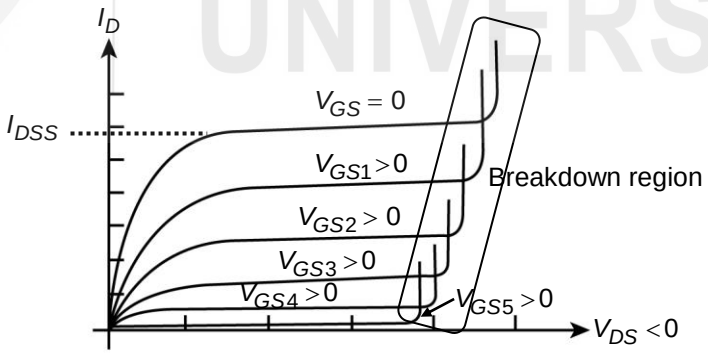



**Fig. 3.23**: **Drain characteristic curve for a *p*-channel JFET.**

9. The JFET is termed a voltage-controlled device because the gate-source voltage $V_{GS}$ controls the flow of drain current in it.

10. When a *p*-channel JFET is "turned off", the saturation current in it becomes zero. When the gate voltage becomes more negative in an *n*-channel JFET, the channel width between the depletion layers decreases.