UNIT 13 ANALOG INTEGRATED CIRCUITS (LINEAR APPLICATIONS)

Structure

13.1 INTRODUCTION

Analog ICs have made present day design of electronic systems quite simple and straightforward. The tough task of biasing the active components like transistors properly has already been taken care of by IC designers. The user has merely to apply the suggested bias supply voltages to the terminals in the IC and the IC is ready for use. Such of these ICs which have currently become popular are the Operational amplifier, Voltage regulator, Comparator, Function generator, Multiplier, Log and Antilog amplifiers and Phase Locked Loops. Even Digital to Analog Converters can be included in this category. This chapter explains the main applications of some of these Analog ICs. Some of the other applications are given in Unit 15. In this unit we shall be restricting ourselves to applications where the opamp is working in the active region, assumed to be linear.

Objectives

After studying this unit, you should be able to explain how to

- multiply voltages by constants either negative or positive and to add or subtract voltages,
- integrate or differentiate voltages,
- regulate dc voltages,
- compress or expand data (voltages) using log or antilog operations, and
- halfwave rectify low valued sinusoidal signals.

13.2 OPERATIONAL AMPLIFIER AND ITS USE IN BASIC NEGATIVE FEEDBACK AMPLIFIERS

The Operational Amplifier popularly known as opamp has replaced the transistor in almost all circuit applications in the low frequency region in the present day circuits. Its characteristics and applications are discussed in this section.

13.2.1 Operational Amplifier

The IC operational amplifier is a high gain stage with differential input and single ended output (with reference to ground). The general purpose operational amplifier has a dc gain of typically 10^5 to 10^6 (100 to 120 dB)** and it is internally frequency

** Communication engineers commonly express voltage or power gain in units called decibels (dB). The basis for this practice is the fact that the human ear has a logarithmic response to the power of the sound impinging on it. It senses the same quantum of increase in the loudness when the power changes from 1 watt to 2 watts as it does when the power changes from 2 watts to 4 watts. In other words, the increase or decrease in loudness sensed by the ear depends on the ratio of powers involved and not on their arithmetic difference. Arising out of this property, a power P_2 is said to be 10 log (P_2/P_1) dB above a power P_1. Relative values of voltages and currents are then specified assuming that the voltages and currents act on the same value of resistance. Thus a voltage gain of V_2/V_1 is expressed in tems of decibels as 10 log $\left(\frac{V_2^2/R}{V_1^2/R}\right)$ or 20 log (V_2/V_1) dB. A voltage or current gain of 10, 100 or 1000 therefore corresponds to 20, 40 and 60 dB respectively. Roughly speaking, the smallest detectable change in loudness by the human ear is about 1 dB.

compensated. As a consequence, its gain reduces at 20 dB per decade upto about 1 MHz. Therefore gain A can be represented as a frequency response function (vide Unit 5) as follows.

$$A(jw) = \frac{A_0}{1 + jw/w_d}$$

and for large w,

$$|A| \simeq \frac{A_0 w_d}{w} = \frac{GB}{w},$$

where A_0 is the d.c. gain, and w_d is the frequency below which frequency response characteristic of the amplifier does not deviate from the dc gain by more than 30%. GB is called the gain-bandwidth product. Typical gain bandwidth product is 1 MHz.

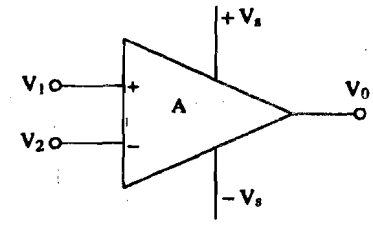

Figure 13.1 (a) : Opamp symbol

Ideal Operational Amplifier

An operational amplifier is indicated by the symbol given in Figure 13.1(a) which shows 5 terminals, the non- inverting and inverting input terminals to which input voltages V_1 and V_2 are applied, the output terminal V_0 and two power supply terminals to whcih $\pm V_S$ volts d.c. are applied. Typically the supply voltage V_S is 10 or 15 Vdc. The opamp has the input-output relation,

$$V_0 = A\,(V_1 - V_2),$$

where as already indicated A has a very large value for low frequencies.

Ideally if $A \to \infty$, $V_1 - V_2 \to 0$ for a *finite output*.

If $V_1 - V_2 \neq 0$ then as $A \to \infty$, $V_0 \to \infty$. However the output voltage V_0 can not exceed the supply voltage V_S and the amplifier output goes to *saturation*. The characteristic of the ideal operational amplifier depicting the situations discussed is shown in Figure 13.1(b).

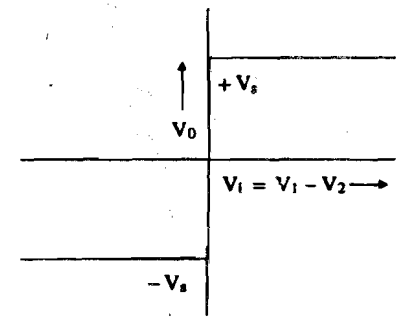

Figure 13.1 (b) : Opamp characteristic

Example 13.1

An opamp has 120 dB gain. If the differential input voltage applied is such that the output is at 10 volts, determine the input voltage.

Solution

Here $20 \log_{10} A = 120$ dB, $\log_{10} A = 6$, Therefore $A = 10^6$

$$\text{Input differential voltage} = \frac{10}{10^6} = 10\,\mu\text{V}.$$

As the above example shows, even for output voltages of the order of volts, the input is of the order of microvolts. **Hence, in practice the assumption that the input terminals of the opamp are almost at the same potential is valid.** If one input terminal is grounded, the other is also at ground potential. This is what is termed **Virtual Ground.**

We shall now proceed to learn some of the important applications of the opamp in electronic circuit design. In Section 13.2.2 to Section 13.2.5, we shall discuss its role in the linear amplification of signals in different modes. Our treatmment in these sections will be in the framework of d.c. signals, but the same equations and results will be valid for time varying input signals as well, provided that at the concerned operating frequencies, A can be considered to be a large real number i.e., for $w < w_d$. Equally the symbols V and I can represent the RMS values of sinusoidal voltages and currents.

SAQ 1

An opamp has a gain of 100 dB. Determine input differential voltage for an output of 1 volt.

13.2.2 Unity Gain Amplifier

In a Unity Gain Amplifier also called a Voltage Follower or a Buffer, the output V_0 is made the same as V_2, one of the inputs to the opamp as shown in Figure 13.2. Then

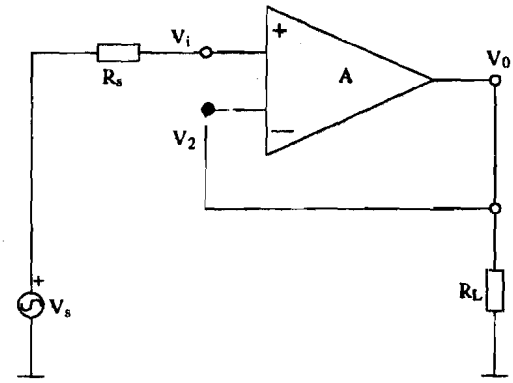

Figure 13.2 : Unity gain amplifier

$$(V_1 - V_2)\,A = V_0$$

$$(V_1 - V_0)\,A = V_0$$

But $$V_1 = V_i$$

Therefore,

$$\frac{V_0}{V_i} = \frac{A}{1+A}$$

As $A \to \infty$, $\frac{V_0}{V_i} \Rightarrow 1$

$V_i = V_S$ as there is no drop in source resistance R_S. Thus $\frac{V_0}{V_S} = 1$.

The amplifier acts as a buffer stage between source and load. The load R_L is driven at the same voltage as the signal source V_S but the signal source is not required to give any output power. Such circuits are useful when the loading of signal sources becomes objectionable.

Example 13.2

An opamp with a gain of 10^6 is used as a unity gain amplifier as shown in Figure 13.2. Determine the actual value of $\frac{V_o}{V_i}$.

Solution

$$\frac{V_o}{V_i} = \frac{A}{1+A} = \frac{1}{1+(1/A)} \approx \left[1 - \frac{1}{A}\right]$$

$$= 1 - \frac{1}{10^6}$$

SAQ 2

An unity-gain amplifier using opamp is found to have $\frac{V_0}{V_i} = 0.999$. Determine the opamp gain A in dB.

13.2.3 Non-inverting Amplifier and Inverting Amplifier

The circuits of Figures 13.2 and 13.3(a) belong to what are called negative feedback circuits i.e. output voltage is feedback to input in such a manner as to oppose the input voltage. The effective input to the amplifier differential terminals gets reduced because of feedback. If the polarities of the amplifier are interchanged, the resulting circuit has positive feedback as shown in Figure 13.3(b).

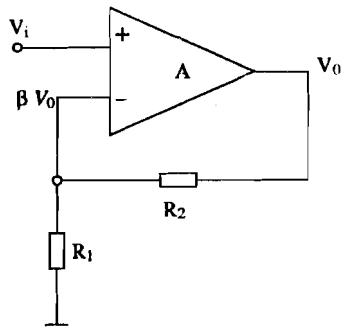

Figure 13.3(a) : Non-inverting amplifier

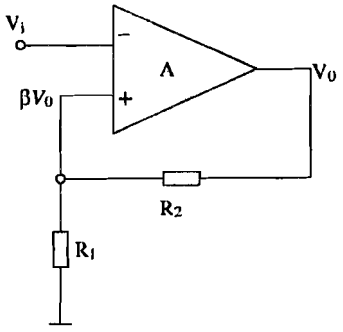

Figure 13.3(b) : Positive feedback amplifier

In the circuit of Figure 13.3(a), $A(V_i - \beta V_0) = V_0$, yielding

$$\frac{V_0}{V_i} = \frac{A}{1 + A\beta},$$

where

$$\beta = \frac{R_1}{R_1 + R_2}.$$

Now when $A \to \infty$, $\frac{V_0}{V_i} = \frac{1}{\beta} = 1 + \frac{R_2}{R_1}$.

This is the nominal value of the gain of the feedback amplifier.

Similar analysis for the circuit of Figure 13.3(b) yields for its gain the following expression

$$\frac{V_0}{V_i} = \frac{-A}{1 - A\beta}$$

In an amplifier design it can be shown that, if $A\,\beta >> 1$ and it is a negative feedback circuit then the amplifier gain is not sensitive to variations in A or one can design amplifiers of stable gain values. Recall the discussion on advantages of negative feedback in Unit 5. It can further be concluded that positive feedback circuits on the other hand become very sensitive to variation in A if $A\beta$ lies between zero and one. However the overall gain of the feedback amplifier gets considerably reduced if one is to satisfy the condition of $A\,\beta >> 1$ in a negative feedback amplifier to maintain acceptable sensitivity factors. Even though a positive feedback amplifier has a higher gain than the original amplifier without feedback, its highly sensitive nature prevents its utility in any practical amplifier design.

The amplifier of Figure 13.3(a) is termed a non-inverting amplifier, as the output V_0 has the same sign as the input V_i. Example 13.4 illustrates the circuit of an inverting amplifier in which V_0 and V_i have opposite signs i.e., a phase reversal occurs in the output for a sinusoidal input.

Example 13.3

A non-inverting amplifier is to be designed for a gain of 100. The opamp gain is 10^6. Design the circuit assuming an ideal opamp of infinite gain and evaluate the percentage error due to the finite gain of opamp.

Solution

The circuit is as shown in Figure 13.3(a).

$$1 + \frac{R_2}{R_1} = 100 : \quad \text{therefore} \quad \frac{R_2}{R_1} = 99.$$

Suitable values of R_2 and R_1 (say 99kΩ and 1kΩ) may then be chosen to conform to this ratio.

If the finite value of A is taken into account,

$$\frac{V_0}{V_i} = \frac{A}{1+A\beta} = \frac{10^6}{1+10^6 \times \frac{1}{100}} = \frac{100}{1+10^4} \approx 100\left(1-\frac{1}{10^4}\right)$$

$$\% \text{ error} = \left(\frac{1}{10^4}\right) \times 100 = 0.01$$

SAQ 3

In the non-inverting amplifier of Figure 13.3(a), $R_2 = 9$ kΩ and $R_1 = 1$ kΩ. Determine the the nominal value of gain and the error if opamp gain is 100 dB.

Example 13.4

Design an inverting amplifier of gain 10.

Solution

If in the circuit of Figure 13.3(a) the + terminal is grounded and input is fed at the end of R_1 where it was earlier grounded, the resulting configuration is an inverting amplifier as shown in Figure 13.4.

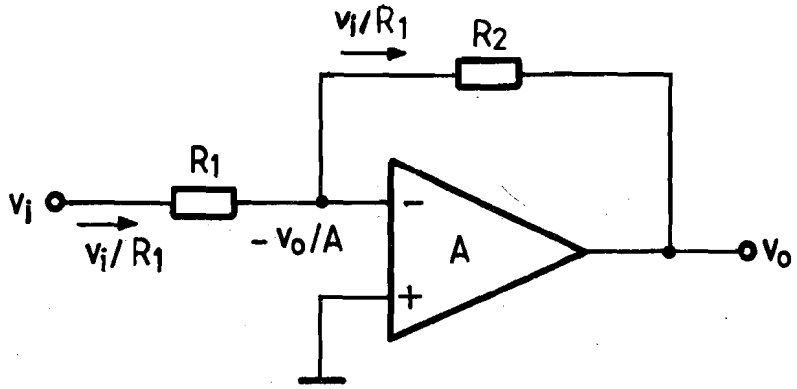

Figure 13.4 : Inverting Amplifier

Using the Kirchhoff's law (current summation at inverting terminal),

$$\frac{V_i}{R_1} + \frac{V_0}{R_2} = \frac{-V_0}{A}\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$$\frac{V_0}{V_i} = \frac{-(R_2/R_1)}{\left[1+\frac{1+(R_2/R_1)}{A}\right]}$$

$$= \frac{-R_2}{R_1} \text{ if } \frac{1+(R_2/R_1)}{A} << 1$$

$$\therefore \frac{R_2}{R_1} = 10, \text{ in the present example.}$$

The currents in R_1 and R_2 would then be as marked in the figure.

SAQ 4

Using the concept of inverting amplifier where the non-inverting terminal is grounded and hence the inverting terminal potential is very nearly at ground potential *(virtual ground)*, design a summing amplifier to sum n voltages.

Example 13.5

Determine the variation in feedback amplifier gain when it has negative feedback with $\beta = 0.09$ and when it has positive feedback, with $\beta = 0.009$. A has a nominal value of 100; it varies from 90 to 110 i.e. by about 10%.

Solution

With $\beta = 0.09$ the negative feedback amplifier has a nominal gain

$$A_f = \frac{100}{1 + 100 \times 0.09} = \frac{100}{10} = 10.$$

As A varies from 100 to 90 (by 10%), A_f changes from 10 to $\frac{900}{91}$.

For the positive feedback situation on the other hand with $\beta = 0.009$,

$$\text{gain } A_f = \frac{-100}{1 - 0.9} = -1000$$

As A changes from 100 to 90, $|A_f|$ changes from 1000 to $\frac{90}{0.19} = 474$.

The graphical representation showing the difference between negative feedback circuit and positive feedback circuit for A and β positive and real is presented in Figures 13.5 and 13.6 respectively.

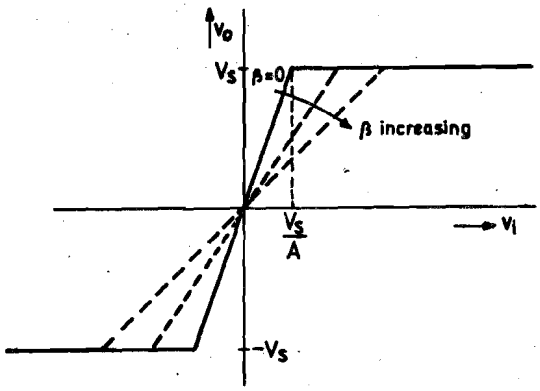

Figure 13.5 : Input-output characteristic for Negative Feedback Circuit

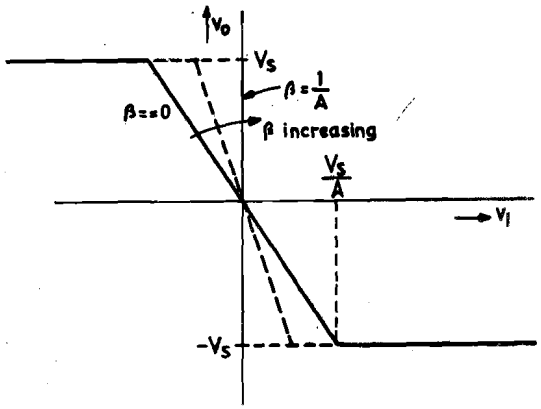

Figure 13.6 : Input-output characteristic for Positive Feedback Circuit

It may be noted that when $\beta = \frac{1}{100}$ and $A = 100$ in the positive feedback circuit of Figure 13.3(b), $A_f \to \infty$ and the characteristic becomes an ideal comparator characteristic changing state from $+V_s$ to $-V_s$ exactly at $V_i = 0$. This circuit is an ideal zero-crossing detector, i.e. it gives an indication at the output by going from high to low state when input voltage v_i crosses zero. Such zero crossing detectors are very useful to close an electronic switch exactly when zero crossing occurs or to cause an operation to be performed after a specific time delay from zero crossover time.

SAQ 5

Determine the variation in gain of a negative feedback amplifier for x % variation in the gain of the opamp, taking β as the feedback factor.

13.2.4 Difference Amplifier

The mathematical operation of subtracting one voltage from the other i.e. $V_0 = V_a - V_b$ is performed by the difference amplifier shown in Figure 13.7.

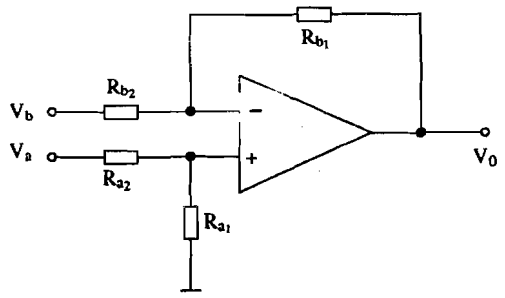

Figure 13.7 : Difference amplifier

Using superposition theorem, on grounding the terminal where V_b is fed the amplifier now becomes a non-inverting amplifier amplifying the voltage $V_a \dfrac{R_{a1}}{R_{a1}+R_{a2}}$ by $\left(1+\dfrac{R_{b1}}{R_{b2}}\right)$. Next grounding the terminal where V_a is fed, the amplifier now becomes an inverting amplifier with gain $\dfrac{-R_{b1}}{R_{b2}}$. Therefore, the resultant output when both the voltages V_a and V_b are applied is

$$V_0 = \frac{V_a R_{a1}}{R_{a1}+R_{a2}}\left(1+\frac{R_{b1}}{R_{b2}}\right) - \frac{R_{b1}}{R_{b2}} V_b.$$

The condition for it to become a difference amplifier is that

$$\left(\frac{R_{a1}}{R_{a1}+R_{a2}}\right)\left(\frac{R_{b2}}{R_{b1}}+1\right) = 1 \text{ or } \frac{R_{b2}}{R_{b1}} = \frac{R_{a2}}{R_{a1}}$$

Under this condition,

$$V_0 = \frac{R_{b1}}{R_{b2}}(V_a - V_b)$$

This result may also be interpreted as follows :

The output of a difference amplifier should be normally due to only the *differential mode signal* $V_d = V_a - V_b$. Therefore the gain $\dfrac{R_{b1}}{R_{b2}}$ is the *differential mode gain* A_d of the difference amplifier. If the condition $\dfrac{R_{b2}}{R_{b1}} = \dfrac{R_{a2}}{R_{a1}}$ is not met, the output may be considered to arise from two components, one the differential mode signal $V_d = V_a - V_b$ and the other what is termed the *common mode signal* $V_c = \dfrac{1}{2}(V_a + V_b)$. Accordingly,

$$V_0 = A_c V_c + A_d V_d \ ,$$

where A_c and A_d are called common mode gain and differential mode gain respectively. The ratio A_d/A_c is termed **common mode rejection ratio** (CMRR) and is a measure of the ability of the difference amplifier to be insensitive to common mode input signals.

$$A_c = \frac{R_{a1}}{R_{a1}+R_{a2}}\left(1+\frac{R_{b1}}{R_{b2}}\right)-\frac{R_{b1}}{R_{b2}}$$

$$A_c = \frac{\left(1-\frac{R_{b1}}{R_{b2}}\cdot\frac{R_{a2}}{R_{a1}}\right)}{\left(1+\frac{R_{a2}}{R_{a1}}\right)}$$

Clearly, $A_c = 0$ if the condition stated earlier for an ideal difference amplifier is met. If for example $R_{b1} = R_{b2} = R_{a1} = R_{a2} = R$, nominally but all the resistors have a tolerance of δ, i.e.

$$R(1-\delta) \le R_x \le R(1+\delta);\ x = a_1, a_2, b_1, b_2$$

then for small δ, $A_d \approx 1$

and
$$A_{c\,(\text{Worst Case})} \approx \frac{1-\frac{(1-\delta)^2}{(1+\delta)^2}}{2}$$

$$\approx \frac{1-\frac{(1-2\delta)}{(1+2\delta)}}{2} \approx \frac{4\delta}{2} = 2\delta$$

$$\text{CMRR}_{\text{(Worst Case)}} = \frac{A_d}{A_c} = \frac{1}{2\delta}$$

Therefore even if we use a very good opamp with very high CMRR, if the resistances used for the difference amplifier have poor tolerance, then the CMRR of the difference amplifier becomes very poor. In order to make the CMRR less dependent on the tolerance of the resistors, an instrumentation amplifier using three operational amplifiers discussed in the next section is used.

Example 13.6

Design a difference amplifier for a gain of 10.

Solution

The circuit is as shown in Figure 13.7.

$$\frac{R_{b1}}{R_{b2}} = 10; \quad \frac{R_{b1}}{R_{b2}} = \frac{R_{a1}}{R_{a2}}$$

Let
$$R_{a2} = R_{b2} = 1\,\text{k}\Omega$$

$$R_{a1} = R_{b1} = 10\,\text{k}\Omega.$$

Example 13.7

If in the above example 1% tolerance components are used, estimate the worst case CMMR.

Solution

For small δ, A_d will be very close to the nominal value, to a first order approximation.

$$A_c = \frac{1-\frac{R_{b1}}{R_{b2}}\cdot\frac{R_{a2}}{R_{a1}}}{1+\frac{R_{a2}}{R_{a1}}}.$$

$$\text{Upper limit of } A_c = \frac{1 - A_d(1-2\delta)\frac{1}{A_d}(1-2\delta)}{1+\frac{1}{A_d}(1-2\delta)}$$

$$\approx \frac{4\delta A_d}{A_d+1}$$

$$\text{Worst Case CMRR} = \frac{A_d}{A_c \text{ (worst case)}} = \frac{A_d+1}{4\delta} = \frac{11}{4\times 0.01} = 275.$$

SAQ 6

Design a difference amplifier for a gain of 100. If 1% components are used estimate the worst case CMRR for the amplifier.

13.2.5 Instrumentation Amplifier

The circuit arrangement of Figure 13.8 shows the three-opamp instrumentation amplifier with the output opamp primarily used as a unity gain difference amplifier.

This amplifier is popularly used as the front-end unit for all instrumentation applications. The special feature about this unit is that the common resistor R_m linking the two inverting terminals of the input operational amplifiers carries only the differential mode current $\frac{V_1 - V_2}{R_m}$. Therefore the outputs V_b and V_a become automatically equal to V_2 and V_1 respectively whenever $V_2 = V_1$ and will be $V_2 - \frac{(V_1 - V_2)}{R_m} R_n$ and $V_1 + \frac{(V_1 - V_2)}{R_m} R_n$ otherwise. Therefore the common mode gain of the overall stage remains the same as that of the difference amplifier but the difference mode gain becomes $1 + \frac{2R_n}{R_m}$ because

$$V_0 = V_a - V_b = \left(V_1 + \frac{(V_1 - V_2)}{R_m} R_n\right) - \left(V_2 - \frac{(V_1 - V_2)}{R_m} R_n\right)$$

$$= \left(1 + \frac{2R_n}{R_m}\right)\left(V_1 - V_2\right)$$

The differential mode gain can be suitably adjusted to the required value by adjusting the single resistor R_m.

Added to the fact that the CMRR now, if δ% tolerance components are used, becomes $\frac{1+\frac{2R_n}{R_m}}{2\delta}$ in the worst case situation, the single element control over the differential mode gain and the buffer action by the unit provide further advantages over the earlier difference amplifier in instrumentation applications.

Example 13.8

An instrumentation amplifier is to be designed for a gain of 100. It uses 1% components. Determine the worst case CMRR.

Solution

The circuit is as shown in Figure 13.8.

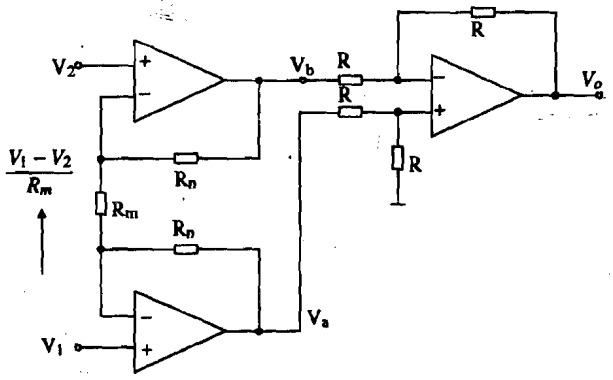

Figure 13.8 : Instrumentation amplifier

$$1 + \frac{2R_n}{R_m} = 100, \text{ so } \frac{R_n}{R_m} = 49.5$$

Let $R_m = 1\,\text{k}\Omega$, therefore $R_n = 49.5\,\text{k}\Omega$.

$$\text{Worst case CMMR} = \frac{100}{2 \times (1/100)} = 5000.$$

SAQ 7

Design an instrumentation amplifier for a gain of 50. For a CMRR (worst case) of better than 5000, estimate the permissible tolerance for the components used.

13.2.6 Integrator and Differentiator

Apart from simple mathematical operations like subtraction and multiplication by a constant performed on voltages, it is necessary to have other linear operations like integration and differentiation performed in order to completely process analog signals linearly.

The element which can be used for this purpose is the capacitor whose terminal relationship $v_c = \frac{1}{C}\int i_c\,dt$ or $i_c = C\frac{dv_c}{dt}$ can be used for integration/differentiation respectively. The operational amplifier is merely used to convert a voltage into a current or a current into a voltage so that the desired relationship occurs for the output voltage with respect to an input-voltage. Figure 13.9 shows the arrangements for an integrator and a differentiator.

For Figure 13.9(a) $v_0 = -v_c = -\frac{1}{C}\int \frac{v_i}{R}\,dt$

$$= -\frac{1}{CR}\int v_i\,dt$$

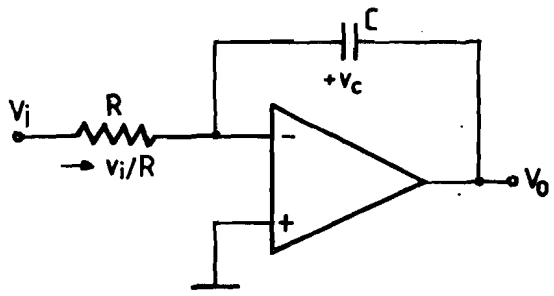

Figure 13.9 (a) : Integrator

For Figure 13.9(b) $v_0 = - v_R = - C(\frac{dv_i}{dt})R = - CR\frac{dv_i}{dt}$

Signal processing when only linear operations are involved is mathematically equivalent to the solution of a set of linear differential equations with certain boundary conditions. All these differential equations can be written in the form of integral equations and circuit arrangements using only integrators can be developed for their simulation. In such application integrators are preferred to differentiators because of the high sensitivity of the output of the differentiators to sudden disturbances (high $\frac{dv_i}{dt}$).

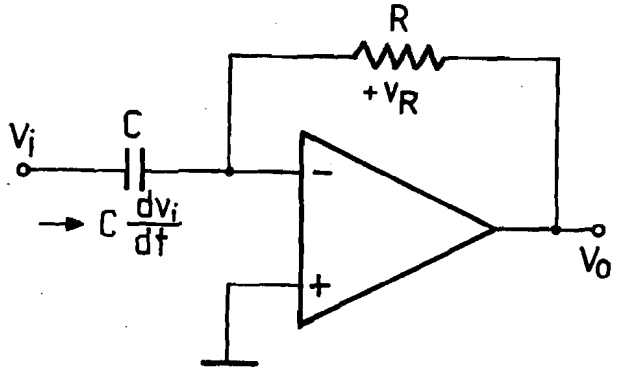

Figure 13.9 (b) : Differentiator

Example 13.9

A dc voltage of 5 V is applied to the integrator circuit of Figure 13.9(a) at $t = 0$. Determine the output voltage if the capacitor is uncharged prior to $t = 0$ and $R = 5\ k\Omega$ and $C = 0.1\ \mu F$.

Solution

The current charging the capacitor after $t = 0$ is

$$= \frac{5V}{5k\Omega} = 1mA$$

Therefore the voltage across the capacitor $= \frac{10^{-3}}{C} t = \frac{10^{-3}}{10^{-7}} t = 10^4 t$

The output voltage $= -10^4\ t$ volts.

It is a ramp with a negative slope of 10^4 volts per second.

SAQ 8

If a square wave of 2.5 V amplitude and 100 kHz is applied to the same integrator, determine its output.

SAQ 9

A sine wave 2.5 sin 100 t volts is applied at the input of the integrator of Example 13.9. Determine its output.

Example 13.10

A square wave of 1 V peak amplitude and 100 kHz frequency is applied to the differentiator circuit of Figure 13.9 (b), having $R = 10\ k\Omega$ and $C = 0.01\ \mu F$. Determine its output.

Solution

Output is a train of positive going and negative going spikes (impulses) occuring at the zero crossing points of the square wave, separated at 5 μ sec.. The amplitude of the spikes is limited by the power supply to the opamp.

SAQ 10

A triangular wave of 2.5 V amplitude and 100 Hz frequency is applied to the differentiator in Example 13.10. Determine its output.

SAQ 11

A sine wave of 1 V peak amplitude and 100 rad/sec is applied to the same differentiator as in SAQ 10. Determine its output.

13.2.7 A Filter Network

Filter networks are widely used in communication engineering and instrumentation to modify the amplitudes of the components of different frequencies in a composite signal. The objective may be to eliminate some unwanted components or to select components falling within a certain band of frequencies or, in general, to manipulate the spectrum (pattern of relative amplitudes of the components) in some desired manner. Traditional filters built of passive circuit elements (*RLC* elements) have yielded place to filters using opamps and *RC* elements (called active *RC* filters) in certain applications, thereby avoiding the need to use inductors which tend to be bulky and loss-prone. In this section, you will be introduced to an example of a simple bandpass filter with a view to provide you with another instance of the versatility of the opamp in analog circuit design and to give you a flavour of active *RC* filter networks.

The passive network arrangement shown in Figure 13.10(a) is a filter called bandpass filter.

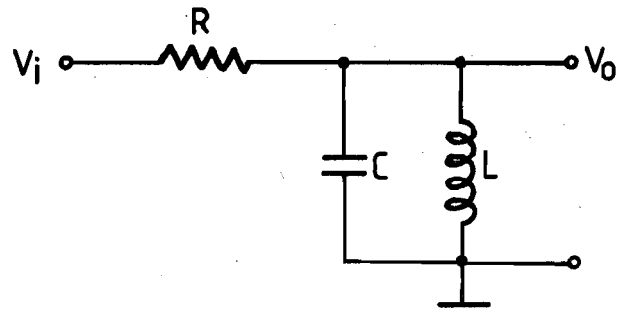

Figure 13.10 (a) : Bandpass Filter

Its frequency response function is given by :

$$\frac{V_0}{V_i} = \frac{\frac{1}{R}}{\frac{1}{R} + j(wC - \frac{1}{wL})}$$

$$= \frac{1}{1 + j(wCR - \frac{R}{wL})}$$

Its magnitude response is plotted in Figure 13.10(b). Note that the output for a given input is appreciable only over a small band of frequencies (called *passband*) of width w_0/Q (called *bandwidth*) centred around a frequency w_0.

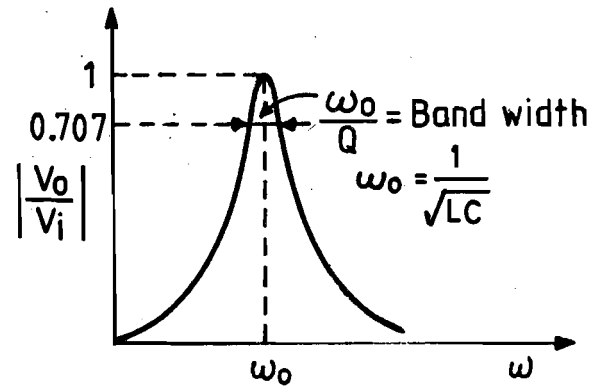

Figure 13.10 (b) : Magnitude Function for a Bandpass Filter made up of RLC
$w_0 = \sqrt{1/LC}$; $Q = R/w_0 L$

The inductor L can be simulated using the circuit of Figure 13.10(c). An analysis of this circuit shows that the section enclosed by the dotted rectangle presents at its input an impedance equal to $jwC(R')^2$ and hence is equivalent to an inductance $L = C(R')^2$. Thus this active RC circuit functions as a bandpass filter with V_i as the input and V_0 as the

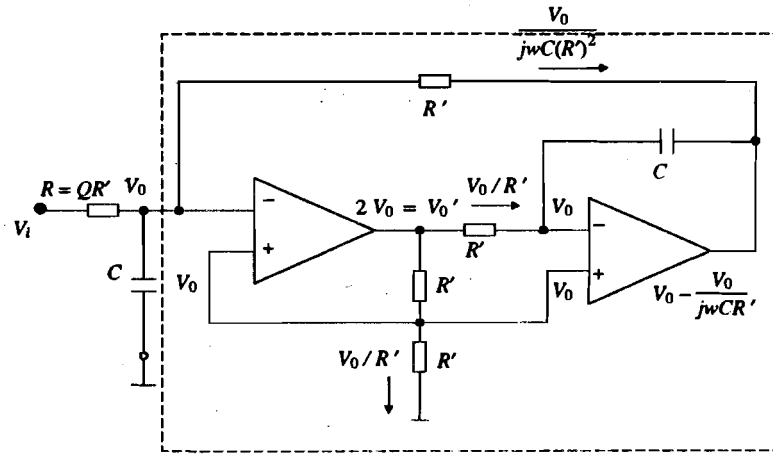

Figure 13.10 (c) : Simulated Inductor

output. Further, $\frac{V_0'}{V_i} = \frac{2V_0}{V_i}$. Therefore V_0' can also be taken as the bandpass filter output and has the added advantage that it is the output of the opamp which means that the output impedance of the filter (Thevenin impedance) is low.

Example 13.11

An active RC bandpass filter is to be designed for a centre frequency of 1000 Hz and a bandwidth of 100 Hz.

Solution

The circuit is as shown in Figure 13.10(c).

$$\frac{R}{R'} = Q = \frac{1000}{100} = 10$$

Let $R' = 1\ \text{k}\Omega\ ;\ R = 10\ \text{k}\Omega$

Now $w_0 = 1/\sqrt{LC} = 1/CR' = 2\pi \times 10^3$

Therefore $$\frac{1}{2\pi \times R'C} = \frac{1}{2\pi \times 10^3\ C} = 10^3$$

$$C = \frac{1}{2\pi \times 10^6} = 0.159\ \mu\text{F}$$

SAQ 12

In the bandpass filter circuit of Figure 13.10(c), $R' = 10\ \text{k}\Omega$, $R = 120\ \text{k}\Omega$ and $C = 0.01\ \mu$ F. Determine the centre frequency and bandwidth.

13.3 VOLTAGE REGULATORS

A dc voltage regulator is a circuit which maintains its output dc voltage constant across a load as either the load current varies or as the input dc voltage varies. You had occasion to learn about a very simple voltage regulator circuit using a zener diode in Unit 11. A dc voltage regulator is an integral component of electronically regulated d.c. power supply units used as standard equipment in the laboratory. It uses a voltage reference, normally a Zener diode reference, a voltage comparator and a series pass transistor. The voltage that is to be maintained is sampled by a resistive divider and compared with the voltage reference using the voltage comparator. The output of the comparator changes or controls the collector emitter voltage drop of the series pass transistor which appears in between the input and output terminals.

13.3.1 Voltage Regulator as a Negative Feedback Control System

The unregulated dc voltage is used as bias voltage to an operational amplifier as shown in Figure 13.11 (a). A voltage reference like that of a Zener diode biased by the unregulated voltage is used as input to the opamp which is used as an amplifier with gain $\left(1 + \frac{R_2}{R_1}\right)$. Therefore the regulated output voltage is $\left(1 + \frac{R_2}{R_1}\right)V_Z = V_0 < V_i$ (unregulated).

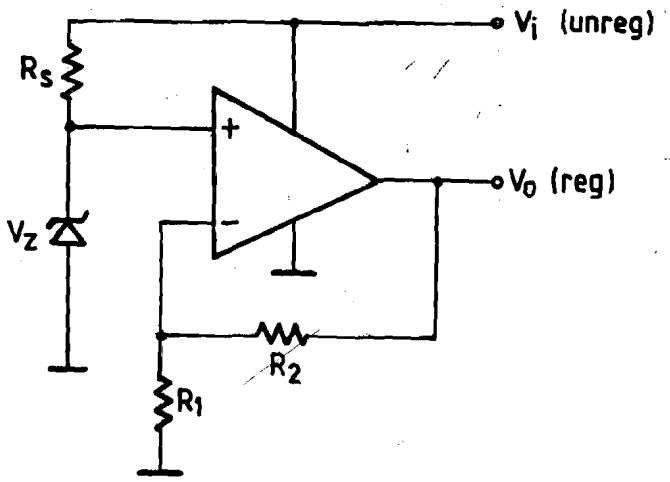

Figure 13.11(a) : Voltage regulator

If the operational amplifier is not capable of delivering the required load current, a current booster may be used as shown in Figure 13.11(b).

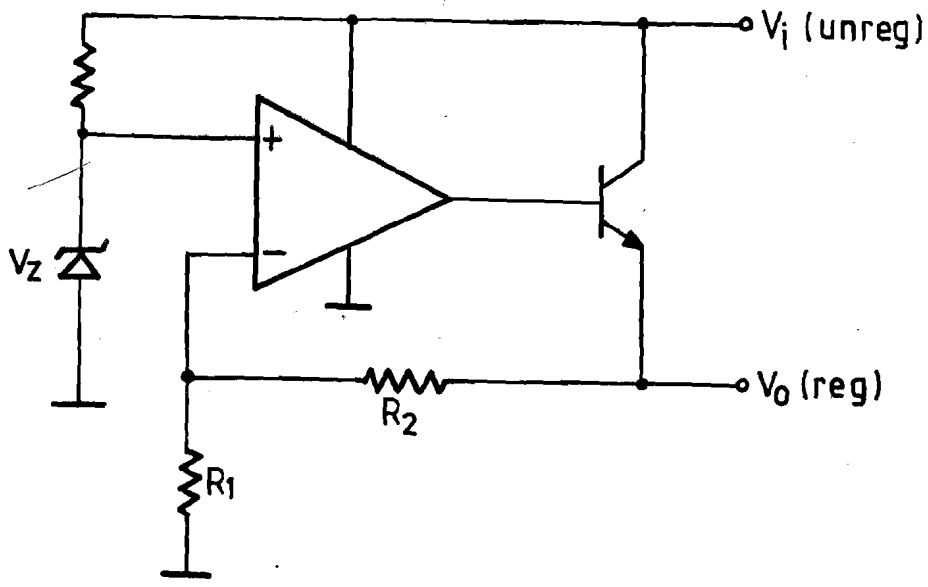

Figure 13.11 (b) : Voltage regulator with current booster

13.3.2 Parameters

The performance of a voltage regulator is measured using the following parameters. **'Line regulation factor'** is defined as the percentage change in nominal output voltage for a stipulated change in input voltage i.e., ($\delta V_0 / V_0$) $\times$ 100 for V_{in} change from $V_{in\ min}$ to $V_{in\ max}$. **'Load regulation factor'** is defined as the percentage change in nominal output voltage for a permisible change in load current i.e., ($\delta V_0 / V_0$) x 100 for I_L changing from 0 to I_{max} .

Temperature coefficient of output voltage is expressed as change in output voltage in ppm per °C change in temperature. **Output impedance** of the regulator is a small signal parameter which is defined as ($-\delta V_0 / \delta I_L$) around nominal V_0 and I_L.

Protection

The voltage regulator being a low output impedance device needs protection against accidental short circuits at the output. Further, as the device acting as pass transistor carries the full load current, there is normally a limitation on the maximum current upto which it can satisfactorily function.

Therefore, the pass transistor has to be protected. This can be done by sensing the load current using a low valued resistor R_{SC} in series with the pass transistor and using the voltage so developed across this resistor to bias a base emitter junction of a transistor and then connecting the collector of this transistor to the base of the pass transistor. This arrangement is shown in Figure 13.12 (a). It will provide a diversion for the extra input

drive base current of the pass-transistor so that the output current remains constant at (V_{BE}/R_{SC}). The voltage regulator characteristics with short circuit protection is shown in Figure 13.12 (b).

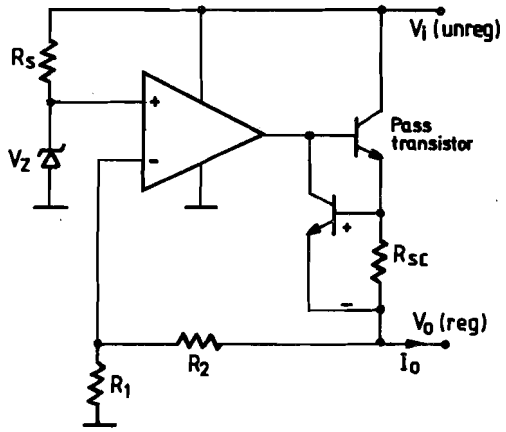

Figure 13.12(a) : Short circuit protection scheme

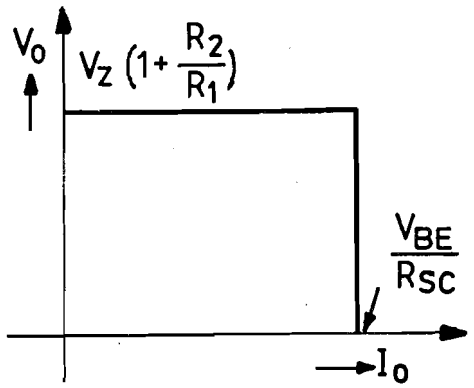

Figure 13.12(b) : Voltage regulator characteristics with short circuit protection

Example 13.12

An opamp regulator as shown in Figure 13.11(a) has a Zener diode with Zener voltage = 5 V, R_S = 1 kΩ. V_i varies from 20 V to 30 V. R_1 = 10 kΩ and R_2 = 20 kΩ. Determine the regulated output voltage across R_L.

Solution

$$\text{Regulated output voltage} = \left(1 + \frac{R_2}{R_1}\right) V_z$$

$$= \left(1 + \frac{20}{10}\right) 5 = 15 \text{ V}$$

Example 13.13

If the opamp in the regulator circuit of Example 13.12 can deliver a maximum current of only 20 mA, what is the limiting value of R_L for which it can function satisfactorily ?

Solution

$$R_{L\,min} = \frac{15}{20} \text{ kΩ} = 750 \text{ Ω}$$

Example 13.14

If the design of Example 13.13 is to be modified for handling loads upto 100 Ω, what is the alteration to be made in the circuit of Figure 13.11(a)?

Solution

The current booster transistor should be introduced between the opamp and the load as shown in Figure 13.11(b). The transistor should be capable of handling more than 15/100 amp or 150 mA of current.

SAQ 13

Design a voltage regulator to deliver 100 mA current at 10 V when the input voltage varies from 15 V to 30 V.

13.4 OTHER APPLICATIONS

The applications in this section use nonlinear elements like diodes in negative feedback configuration of the opamp for certain nonlinear signal processing tasks.

13.4.1 Log , Antilog Amplifiers

The volt-ampere characteristic of a semiconductor diode is known to be exponential. This can be used to obtain log, antilog amplifiers.

For the log amplifier shown in Figure 13.13(a).

$$i_d = \frac{v_i}{R} = I_s\left(\exp\left(\frac{v_d}{V_T}\right) - 1\right)$$

$$\approx I_S \exp\left(\frac{v_d}{V_T}\right)$$

$$v_0 = -v_d = -V_T \ln\left(\frac{v_i}{I_s R}\right)$$

For the antilog amplifier shown in Figure 13.13(b)

$$v_0 = -R\, i_d$$

But

$$i_d = I_S\left(\exp\left(\frac{v_d}{V_T}\right) - 1\right)$$

$$i_d \approx I_S \exp\left(\frac{v_i}{V_T}\right)$$

$$v_0 = -i_d R$$

$$= -I_S R \exp\left(\frac{v_i}{V_T}\right)$$

Since exponentiation is equivalent to antilog operation, this is called an antilog amplifier.

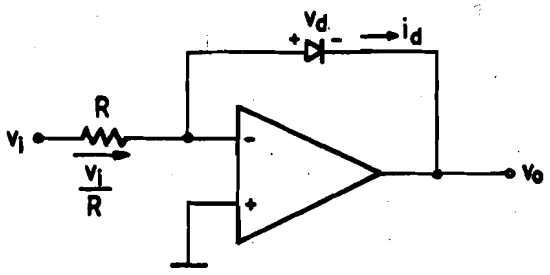

Figure 13.13(a) : Log Amplifier

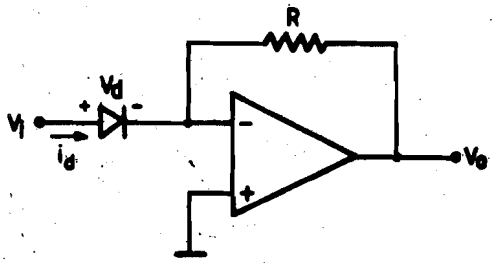

Figure 13.13(b) : Antilog Amplifier

Example 13.15

Design a multiplier using log-antilog amplifiers. Use diodes with identical characteristics (i.e., I_S is the same for all diodes).

Solution

The circuit for multiplying two voltages v_x and v_y is shown in Figure 13.13(c). The outputs of the two log amplifiers are $-V_T \ln (v_x / I_S R_x)$ and $-V_T \ln (v_y / I_S R_y)$. The output of the summing amplifier is $V_T[\ln (v_x / I_S R_x) + \ln (v_y / I_S R_y)] = V_T \ln\left(\frac{v_x v_y}{I_S^2 R_x R_y}\right)$. As this forms the input to the

antilog amplifier, its output would be

$$-I_S R \exp\left(V_T \ln \frac{v_x v_y}{I_S^2 R_x R_y}/V_T\right) = -\frac{R v_x v_y}{I_S R_x R_y} = K_m v_x v_y, \text{ where } K_m = -R/I_S R_x R_y.$$

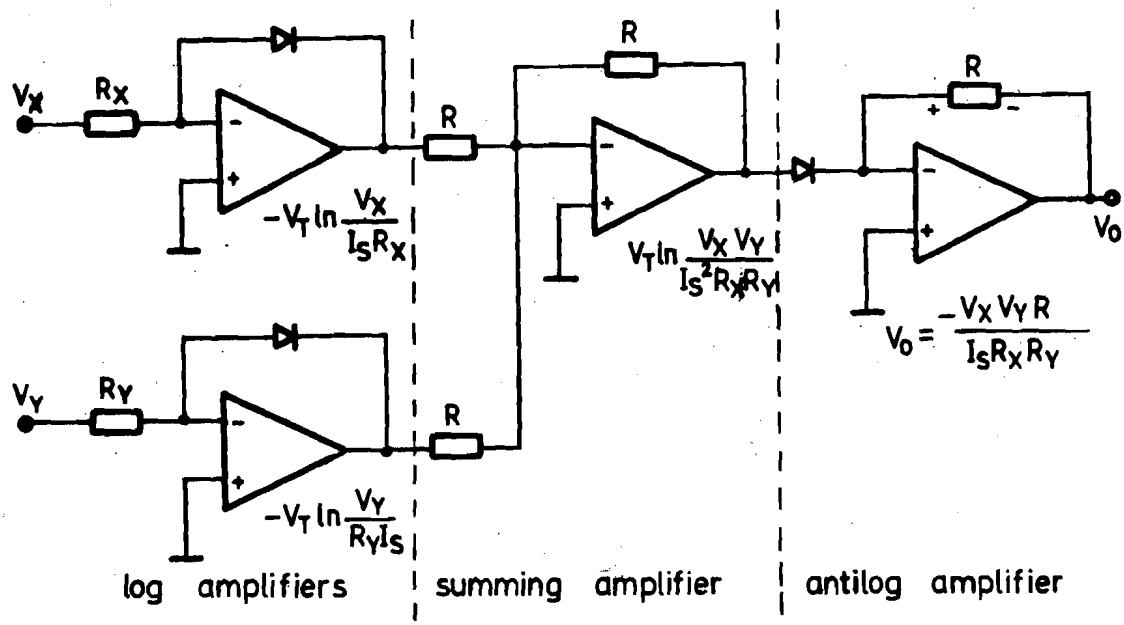

Figure 13.13(c) : Multiplier

SAQ 14

Design a divider using log-antilog amplifiers.

13.4.2 Precision Rectifier

In simple rectifier circuits employing silicon diodes (vide Unit 11), the output is less than the ideal value by the nonlinear voltage drop across the diode. Furthermore, such circuits can not rectify low level a.c. voltages (typically of less than 0.7 V peak value). By using opamps in conjunction with diodes, these limitations can be overcome. In this section, we shall discuss such arrangements, which go by the name of precision rectifier circuits.

In the circuit shown in Figure 13.14, D_1 conducts during the positive half of the input cycle and D_2 conducts during the negative half of the input and the output v_{01} is as shown in Figure 13.14.

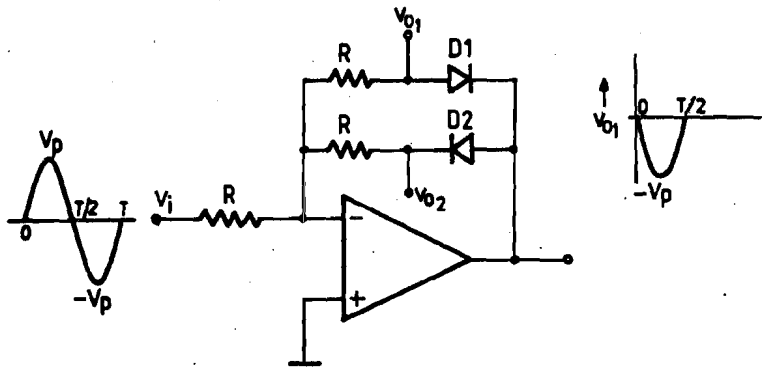

Figure 13.14 : Precision Rectifier Circuit

Example 13.16

In the precision rectifier circuit of Figure 13.14, sketch the output v_{02}.

Solution

Diode D_2 conducts, during the negative half-cycle of the input, giving rise to the output voltage v_{02} sketched in Figure 13.15.

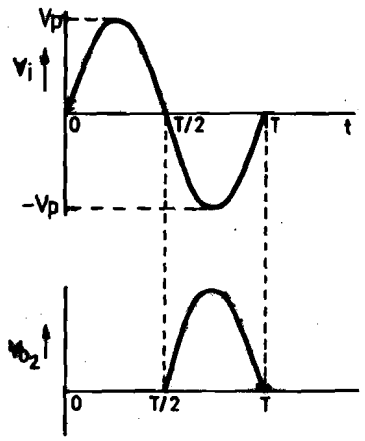

Figure 13.15 : For solution to Example 13.16

SAQ 15

Design a full wave rectifier (precision) using opamps.

Precision rectifiers have a number of applications in communication engineering and instrumentation. For example, the full wave rectifier circuit of SAQ 15 can be used to measure the absolute average value of a periodic waveform. All that needs to be done for this purpose is to connect a d.c. voltmeter to the output of this circuit and take its reading.

13.5 SUMMARY

This unit dealt with the use of an operational amplifier for mathematical operations like multiplying by a constant, adding, subtracting, integrating, differentiating and filtering analog signals. Regulation of dc voltages and rectification of low valued sinusoidal voltages performed with the help of opamps are the other signal processing activities treated here. Multiplication and division of voltages are also discussed.

On completion of a study of this unit, you would no doubt have gained an appreciation of the role of the opamp in modern analog electronic circuit design.

13.6 ANSWERS TO SAQs

SAQ 1

$100 \text{ dB} = 20 \log A$

$A = 10^5$

Input differential voltage $= \dfrac{1\text{V}}{10^5} = 10\,\mu\text{V}.$

SAQ 2

$$\frac{V_0}{V_i} = \frac{A}{1+A} = 0.999$$

$$0.999 + 0.999\,A = A$$

$$A = 999$$

Gain in dB $= 20 \log_{10} 999 \approx 60$

SAQ 3

$$\text{Gain} = 1 + \frac{R_2}{R_1} = 1 + \frac{9}{1} = 10$$

$$20 \log_{10} A = 100, \quad A = 10^5$$

$$\text{Therefore actual gain} = \frac{10^5}{\left(1 + 10^5 \times \frac{1}{10}\right)} = \frac{10^5}{\left(1 + 10^4\right)}$$

$$\approx 10\left(1 - \frac{1}{10^4}\right)$$

$$\% \text{ error} = \frac{1}{10^4} \times 100 = 0.01$$

SAQ 4

The circuit is shown in the figure. It is clear from the figure that the sum of the input currents $[V_{ik}/R_k]$ is passed through R, yielding an output V_o which is the weighted sum of the input voltages. The coefficient of the input voltage V_{ik} in this sum is $-(R/R_k)$.

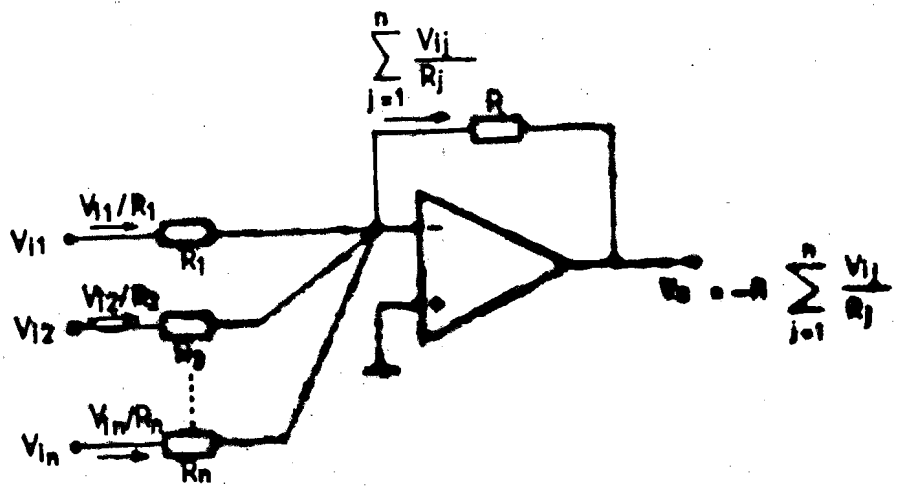

Figure for Answer to SAQ 4

SAQ 5

A_f, gain after feedback $= \dfrac{A}{1+A\beta}$

$$\frac{\delta A}{A} = \frac{x}{100}$$

$$\frac{\delta A_f}{\delta A} = \frac{1}{1+A\beta} - \frac{A\beta}{(1+A\beta)^2}$$

$$= \frac{1}{(1+A\beta)^2}$$

$$\frac{\delta A_f}{A_f} = \frac{\delta A_f}{\delta A}\frac{\delta A}{A_f} = \frac{\delta A_f}{\delta A}\frac{\delta A}{A}\frac{A}{A_f}$$

$$= \frac{1}{(1+A\beta)} \times \frac{x}{100}$$

$$= \frac{(x/100)}{1+A\beta}$$

Note that the percentage variation of the overall amplifier gain is reduced by a factor $(1 + A\beta)$ as compared with an amplifier without negative feedback.

SAQ 6

$\frac{R_{b1}}{R_{b2}} = 100$ in Figure 13.7.

Choose $R_{b1} = R_{a1} = 100\ \text{k}\Omega$; $R_{a1} = R_{b2} = 1\text{k}\Omega$

Worst case CMRR $= \frac{A_d + 1}{4\delta} = \frac{101}{4 \times 0.01} = 2525.$

SAQ 7

$1 + \frac{2R_n}{R_m} = 50$ in Figure 13.8.

$\frac{R_n}{R_m} = 24.5.$ Let $R_m = 1\ \text{k}\Omega.$

$R_n = 24.5\ \text{k}\Omega.$

Worst case CMRR $= \frac{50}{2\delta} > 5000$

$\delta \leq \frac{1}{200}$ or better than 0.5%.

SAQ 8

The output voltage increases linearly with a slope of $\frac{2.5}{CR}$ V/s during the negative half cycle of the square wave and decreases linearly with the same slope during the positive half cycle. Therefore the output is a triangular wave with a peak to peak voltage of

$$\frac{2.5}{CR} \times \frac{T}{2} = \frac{2.5 \times 10 \times 10^{-6}}{5 \times 10^3 \times 10^{-7} \times 2} = 25\ \text{mV}$$

Peak value of the triangular voltage = 12.5 mV

SAQ 9

Output $= \frac{2.5}{100 \times CR} \cos 100t$

$$= \frac{2.5 \cos 100t}{100 \times 5 \times 10^3 \times 10^{-7}}$$

$$= 50 \cos 100t\ \text{V}$$

SAQ 10

The triangular wave rises or falls with a slope of magnitude $\left(\frac{2.5}{T/4}\right)$ V/s during successive half cycles.

Output therefore is a square wave of amplitude

$$= RC\left(\frac{2.5}{T/4}\right)$$

$$= 10 \times 10^3 \times 10^{-8} \left(\frac{2.5}{T/4} \right)$$

$$= 10^{-4} \times \frac{2.5 \times 4}{(1/100)}$$

$$= 0.1 \text{ V}$$

SAQ 11

$$\text{Output} = -wRCV_p \cos wt$$

$$= -100 \times 10^4 \times 10^{-8} \times 1 \cos 100\, t$$

$$= -10^{-2} \cos 100t \text{ volts}$$

SAQ 12

$$\text{Centre frequency} = \frac{1}{2\pi R' C}$$

$$= \frac{1}{2\pi \times 10^4 \times 10^{-8}} \text{ Hz}$$

$$= 1.591 \text{ kHz.}$$

$$Q = \frac{120}{10} = 12.$$

$$\text{Bandwidth} = \frac{1591}{12} \text{ Hz}$$

$$= 132.6 \text{ Hz.}$$

SAQ 13

Assume that the opamp can deliver 100 mA current.

The circuit is as shown in Figure 13.11(a) with

$$5 \left(1 + \frac{R_2}{R_1} \right) = 10$$

$$\frac{R_2}{R_1} = 1. \quad \text{Let } R_1 = R_2 = 10\,\text{k}\Omega.$$

SAQ 14

Division corresponds to subtraction in logarithmic domain. Hence we use a difference amplifier instead of a summing amplifier in the multiplier circuit of Figure 13.13(c). The resulting divider circuit is shown in the accompanying figure.

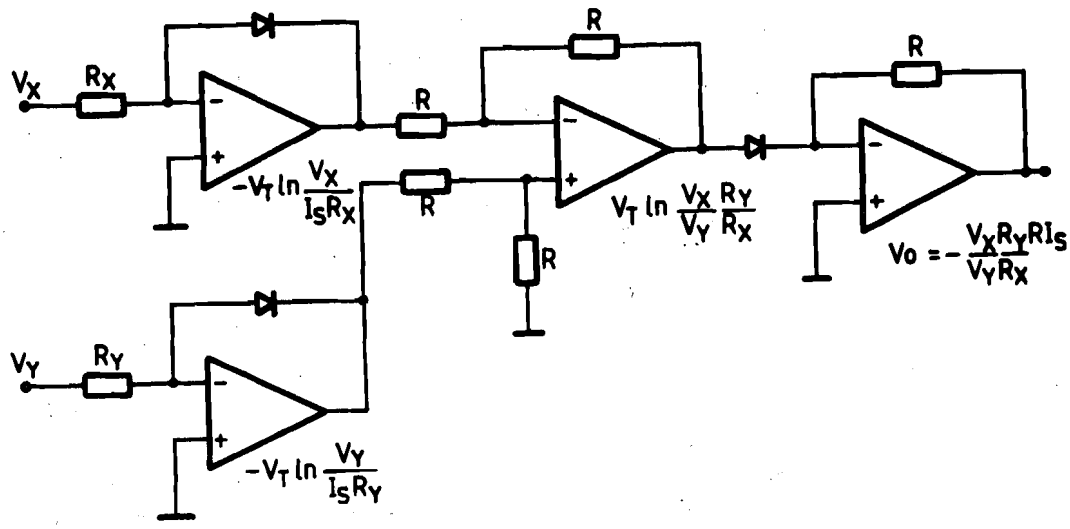

Figure for Answer to SAQ 14 : Divider using log-antilog amplifiers

SAQ 15

If v_{01} and v_{02} of Figure 13.14 are given to a difference amplifier, as shown in the accompanying figure, the output is $v_{02} - v_{01} = |v_i|$, which is a full-wave rectified version of the input.

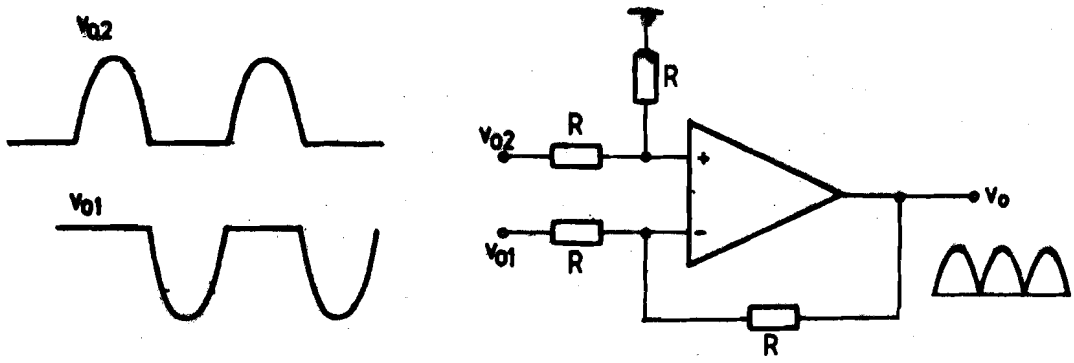

Figure for Answer to SAQ 15 : Full wave precision rectifier